SM563
4-Bit Single-Chip Microcomputer

FEATURES

- 4,096 × 8-bits ROM Capacity
- 160 × 4-bits RAM Capacity
  (Including 32 × 4-bits Display RAM)
- 98 Instruction Sets
- A RAM Area is Used as Stack Area
- I/O Ports
  - 4 Input
  - 11 Input/Output plus 15 also used as LCD Segment Port)
- Interrupts
  - Internal Interrupt × 4 (Timer/Counter, f4 Signal, Serial I/O, Divider Overflow)
  - External Interrupt × 1 (P0 Signal)
- Timer/Counter 8-bits × 1
- Serial Interface 8-bits × 1
- Built-in Main Clock Oscillator for System Clock
- Built-in Sub Clock Oscillator for Real Time Clock
- Built-in 15 Stages Divider for Real Time Clock
- Built-in LCD Driver
  - 128 Segments
  - 1/3 Bias
  - 1/4 Duty Cycle (If LCD Drive CIrcuit is Used, a Crystal Oscillator Circuit Needs to be Constituted Between OSC_{IN} and OSC_{OUT})
- Instruction Cycle Time
  - 6.67 µs (TYP., 600 Hz at 3 V)
  - 2 µs (MIN., 2 MHz at 5 V)
- Buzzer Output
- Standby Function
- Supply Voltage 2.7 V to 5.5 V
- 64-pin QFP (QFP064-P-1420) Package

DESCRIPTION

The SM563 is a CMOS 4-bit single-chip microcomputer incorporating 4-bit parallel processing function, ROM, RAM, I/O ports, serial interface, and timer/counter in a single chip.

It provides five kinds of interrupt and subroutine stack function using the RAM area. Provided with a 128 segments LCD drive circuit, this microcomputer is suitable for low power systems with multiple LCD segments.

PIN CONNECTIONS

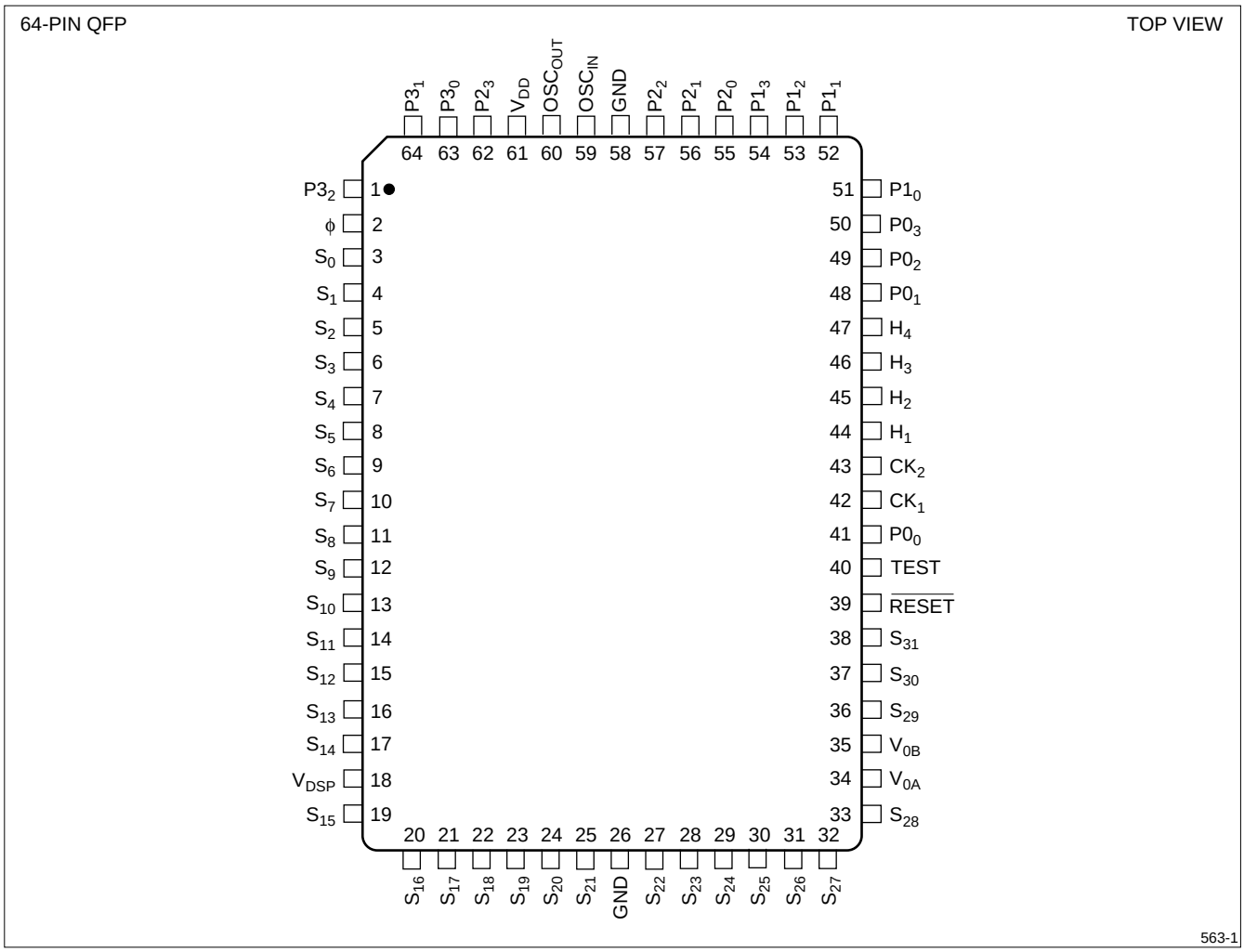
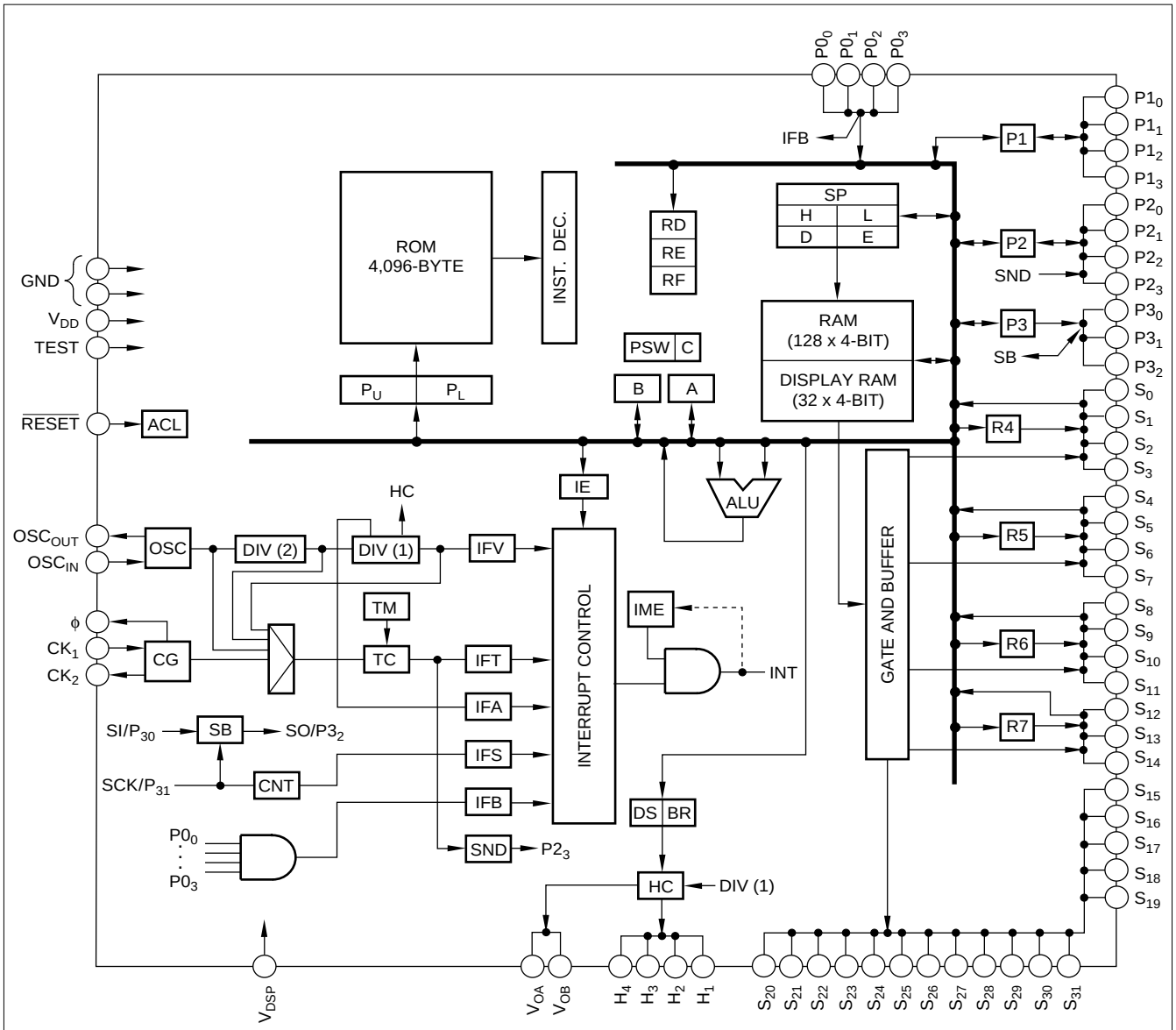


Figure 1. 64-pin QFP



NOTE: Symbol Description

A, B: Accumulators
ACL: Auto clear
ALU: Arithmetic logic unit
BR, DS: Common signal control F/F
CG: Clock generator
DIV: Divider
D, E, H, L: General-purpose registers
HC: Common signal circuit
IE: Interrupt enable F/F
IFA, IFB, IFS, IFT, IFV: Interrupt requests
IME: Interrupt master enable F/F
P1 - P3: Registers
P_L, P_U: Program counters
PSW: Program status word register
R4-R7: General-purpose registers
RD, RE, RF: Mode registers
SB: Shift register
SP: Stack pointer
TC: Count register
TM: Modulo register

563-2

Figure 2. Block Diagram

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
$P0_0$ - $P0_3$	I	$A_{CC} \leftarrow P0_0$ - $P0_3$, with pull-up resistor
$P1_0$ - $P1_3$	I/O	I/O selectable by instructions, with pull-up resistor
$P2_0$ - $P2_3$	I/O	I/O selectable independently, with pull-up resistor. Sound output only when $P2_3$ pin is used as an output
$P3_0$ - $P3_2$	I/O	Serial interface I/O by setting the mode register RE, with pull-up resistor
S_0 - S_{14}	O or I/O	Selectable between segment ports and I/O ports through an RC register
S_{15} - S_{31}	O	Display RAM contents output as LCD segment signals
H_1 - H_4		4-value output capability; used for LCD common output
TEST	I	For test (connected to GND normally), with pull-down resistor
$\overline{RESET}$	I	Auto clear, with pull-up resistor
ϕ	O	System clock output
CK_1, CK_2		For system clock oscillation
OSC_{IN}, OSC_{OUT}		For clock oscillation
V_{DSP}, V_{OA}, V_{OB}		Power supply for LCD driver
V_{DD}, GND		Power supply for logic circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply Voltage	V_{DD}	-0.3 to +7	V	1
	V_{DSP}	-0.3 to +7	V	1
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V	1
Output Voltage	V_{OUT}	-0.3 to V_{DD} + 0.3	V	1
Output Current	I_{OUT}	20	mA	2
Operating Temperature	T_{OPR}	-20 to +70	°C	
Storage Temperature	T_{STG}	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Sum of current from (or flowing into) output pins.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply Voltage	V_{DD}		2.7		5.5	V	
	V_{DSP}		2.7		V_{DD}	V	
Basic Oscillation Frequency	f	V_{DD} = 2.7 V to 5.5 V	250		600	kHz	1
		V_{DD} = 4.5 V to 5.5 V	250		2,000	kHz	1
Instruction Cycle	t	V_{DD} = 2.7 V to 5.5 V	6.7		16	µs	
		V_{DD} = 4.5 V to 5.5 V	2		16	µs	
Crystal Oscillation Frequency	f_{OSC}			32.768		kHz	

NOTE:
1. Frequency fluctuation: ±30%.

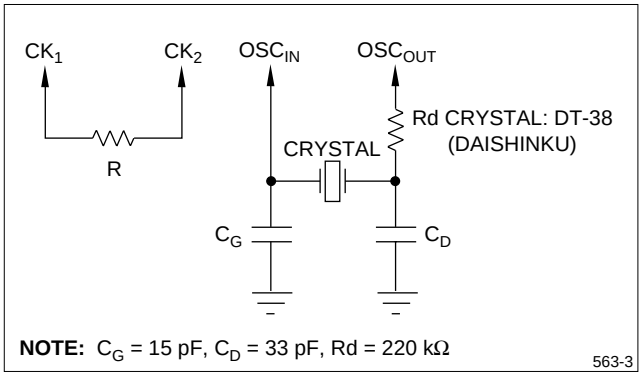


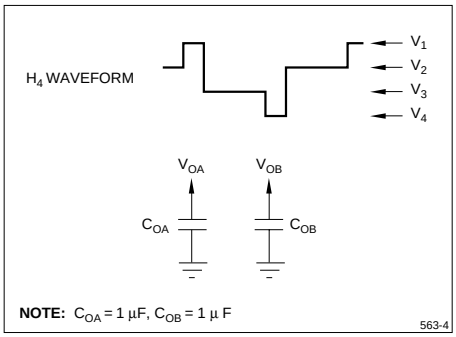
Figure 3. Oscillation Circuit

DC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, T_{OPR} = -20°C to +70°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	V_{IH1}		0.7 × V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.3 × V_{DD}	V	1
	V_{IH2}		V_{DD} – 0.5		V_{DD}	V	2
	V_{IL2}		0		0.5	V	2
Input Current	I_{IH}	V_{IN} = 0 V,	2		200	µA	1
		V_{DD} = 4.5 V to 5.5 V	20		200	µA	1
Output Current	I_{OH1}	V_{OH} = V_{DD} – 0.5 V	50			µA	3
	I_{OL1}	V_{OL} = 0.5 V	250			µA	3
	I_{OH2}	V_{OH} = V_{DD} – 0.5 V	5		250	µA	4
	I_{OL2}	V_{OL} = 0.5 V	500			µA	4
	I_{OH3}	V_{OH} = V_{DD} – 0.5 V	100			µA	5
		V_{DD} = 4.5 V to 5.5 V	400			µA	5
	I_{OL3}	V_{OL} = 0.5 V	0.5			mA	5
		V_{DD} = 4.5 V to 5.5 V	1.6			mA	5
Output Impedance	R_C			5	20	kΩ	6
	R_S			10	40	kΩ	7
Output Voltage	V_1	V_{DSP} = 3.0 V, No load	2.7		3	V	8
	V_2		1.7	2	2.3	V	8
	V_3		0.7	1	1.3	V	8
	V_4		0		0.3	V	8
Supply Current	I_{OP}	f = 600 kHz, V_{DD} = 3.0 V		0.4	1.5	mA	9
	I_{SB}	Standby current V_{DSP} = 3.0 V		15	40	µA	10
		Standby current V_{DD} = 3.0 V		8	20	µA	11

NOTES:
1. Applicable pins: $P0_0$ - $P0_3$, $\overline{RESET}$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P3_0$ - $P3_2$, (during input mode).
2. Applicable pins: CK_1, TEST, OSC_{IN}.
3. Applicable pin: CK_2.
4. Applicable pins: $P1_0$ - $P1_3$ (during output mode).
5. Applicable pins: $P2_0$ - $P2_3$, $P3_0$ - $P3_2$ (during output mode), ϕ.
6. Applicable pins: H_1 - H_4.
7. Applicable pins: S_0 - S_{31}.
8. Applicable pins: H_1 - H_4, S_0 - S_{31}.
9. No load condition.
10. No load condition when bleeder resistance is ON.
11. No load condition when bleeder resistance is OFF.



PIN FUNCTIONS

GND, V_{DD}, V_{DSP} (Power Supply Inputs)

Both GND pins 26 and 58 should be grounded. The V_{DD} pin is the positive power supply with respect to GND. The V_{DSP} is the positive power supply for a LCD driver with respect to GND.

TEST (Test Input)

The TEST pin should be left open or connected to GND with a pull-down resistor.

$\overline{\text{RESET}}$ (Input)

The $\overline{\text{RESET}}$ accepts an active low system reset which initializes the iternal logic of the device. Normally a capacitor of about 0.1 µF is connected between this pin and GND to provide a power on reset function.

OSC_{IN}, OSC_{OUT} (Crystal Oscillator Pins)

The OSC_{IN} and OSC_{OUT} pins connect with an external crystal oscillator and these pins and the GND connect with a capacitor, which constitute an oscillator circuit.

The output of the oscillator is coupled to a clock divider for real-time clock operation.

CK_1, CK_2 (System Clock CR Oscillator Pins)

The CK_1 and CK_2 pins, in conjunction with a resistor between them, provide a system clock oscillator.

H_1 to H_4 (Common Signal Outputs)

The H_1 to H_4 pins are used to drive the common of a LCD.

S_0 to S_{31} (Segment Outputs)

The S_0 to S_{31} pins drive LCD segments. Pins S_0 through S_{14} may also be used as I/O ports when specified with the mode register RC.

$P0_0$ to $P0_3$ (Inputs)

The P0 pins are normally used to accept key input data. A falling edge at these pins resets the IFB flag.

$P1_0$ to $P1_3$ (Input/Output)

The P1 are I/O pins connected to the positive supply with pull-up resistors. They may be switched between input and output modes through an instruction.

$P2_0$ to $P2_3$ (Input/Output)

The $P2_0$ to $P2_3$ pins are bit-independent I/O ports which can be independently set to input or output mode with the mode register RF.

When the $P2_3$ is used for an output pin, it serves exclusively as a sound output pin, which can output a sound signal with any frequency set up by the timer counter.

Pins $P2_0$ and $P2_1$ output the Od and R/W signals with the mode register RC.

$P3_0$ to $P3_2$ (Input/Output)

The $P3_0$ to $P3_2$ pins are I/O pins which are connected to the positive supply with pull-up resistors. These pins can be set to I/O mode for use in a serial interface with the mode register RE.

SYSTEM CONFIGURATION

ROM and Program Counter

The on-chip ROM has a configuration of 64-page × 64-step × 8-bit, and stores programs and table data.

The program counter consists of a 6-bit page address counter P_U and 6-bit binary counter P_L used to specify the steps within a page.

The locations shown in Figure 3 are allocated in the on-chip ROM.

Stack Pointer (SP)

The stack pointer (SP) is an 8-bit shift register which holds the starting address of the stack area of RAM space. Immediately after the reset, the contents of the stack pointer are uninitialized and must be set to an appropriate value. If, for instance, the initial value of the stack pointer is set to 80_H, the data memory is beginning with the highest address (excluding the display RAM area). $7F_H$ is usable as a stack area.

RAM

Data memory has a 160-word × 4-bit configuration, and is used to store processing data and other information. Data memory is also used as a stack area to save register values, the program counter value and program status word (PSW) at the time a subroutine jump or an interrupt occurs. Figure 4 shows the RAM configuration. 2 × 16 × 4-bit of entire RAM space is used as a display RAM area from which data is output to LCD segment driving pins. A LCD with a 1/4 duty and 1/3 bias format can be directly driven by writing display data into the display RAM area. The display RAM outputs are, as shown in Figure 5, connected to segment output pins S_0 to S_{31} for individual set of common outputs H_1 to H_4. The segment output pins provide a single digit of display RAM data M_0 to M_3, as a LCD driving waveform signal according to H_1 to H_4 outputs. The operations of the display RAM are identical to those of other RAM areas.

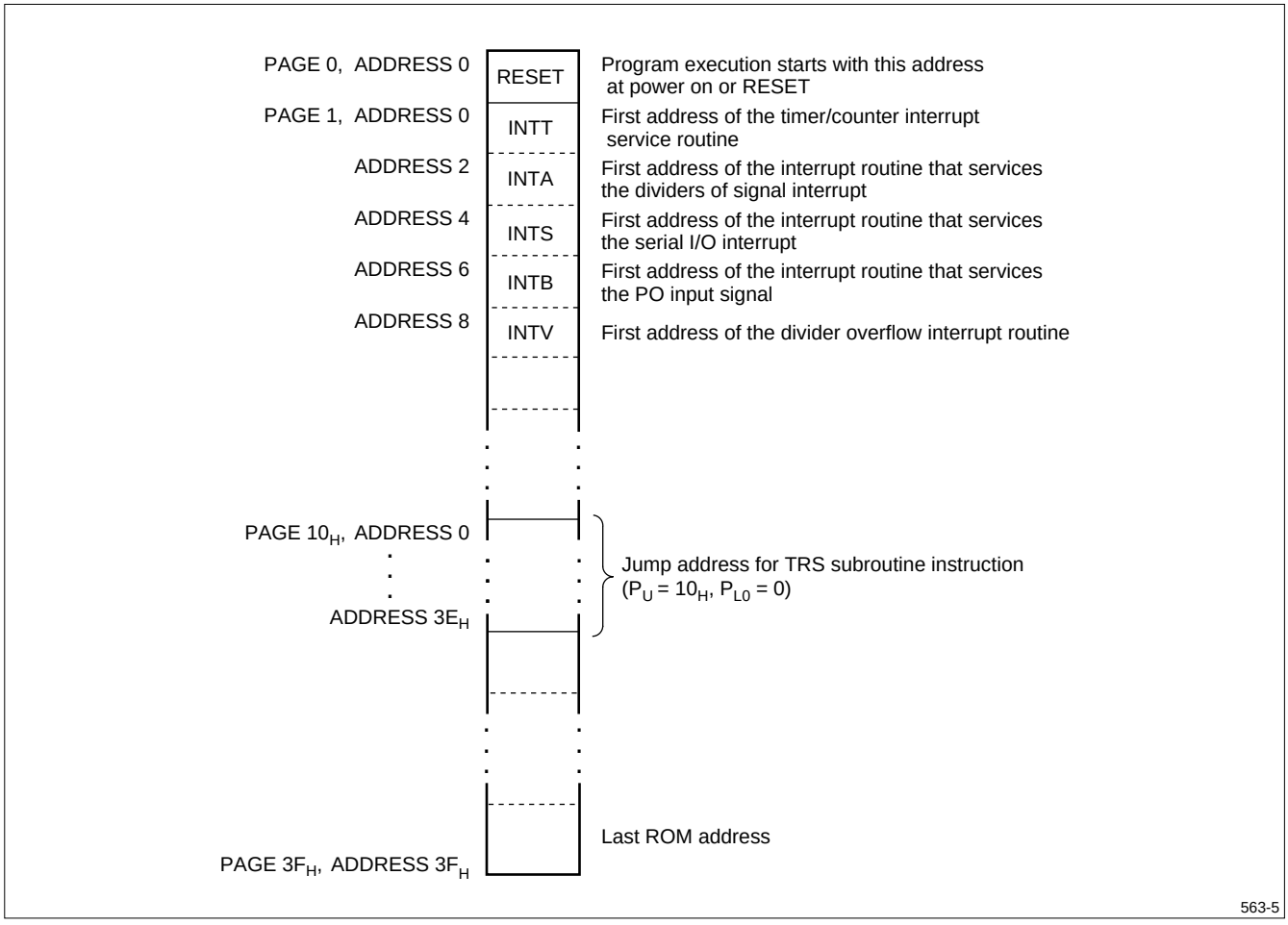


Figure 4. Program ROM Map

L \ H	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001
0000									S_0	S_{16}
0001									S_1	S_{17}
0010									S_2	S_{18}
0011									S_3	S_{19}
0100									S_4	S_{20}
0101									S_5	S_{21}
0110									S_6	S_{22}
0111									S_7	S_{23}
1000									S_8	S_{24}
1001									S_9	S_{25}
1010									S_{10}	S_{26}
1011									S_{11}	S_{27}
1100									S_{12}	S_{28}
1101									S_{13}	S_{29}
1110									S_{14}	S_{30}
1111									S_{15}	S_{31}

NOTE: The area with the thick is allocated for a display RAM and the Sn (n = 0 to 31) shows the related segment outputs.

Figure 5. RAM Configuration

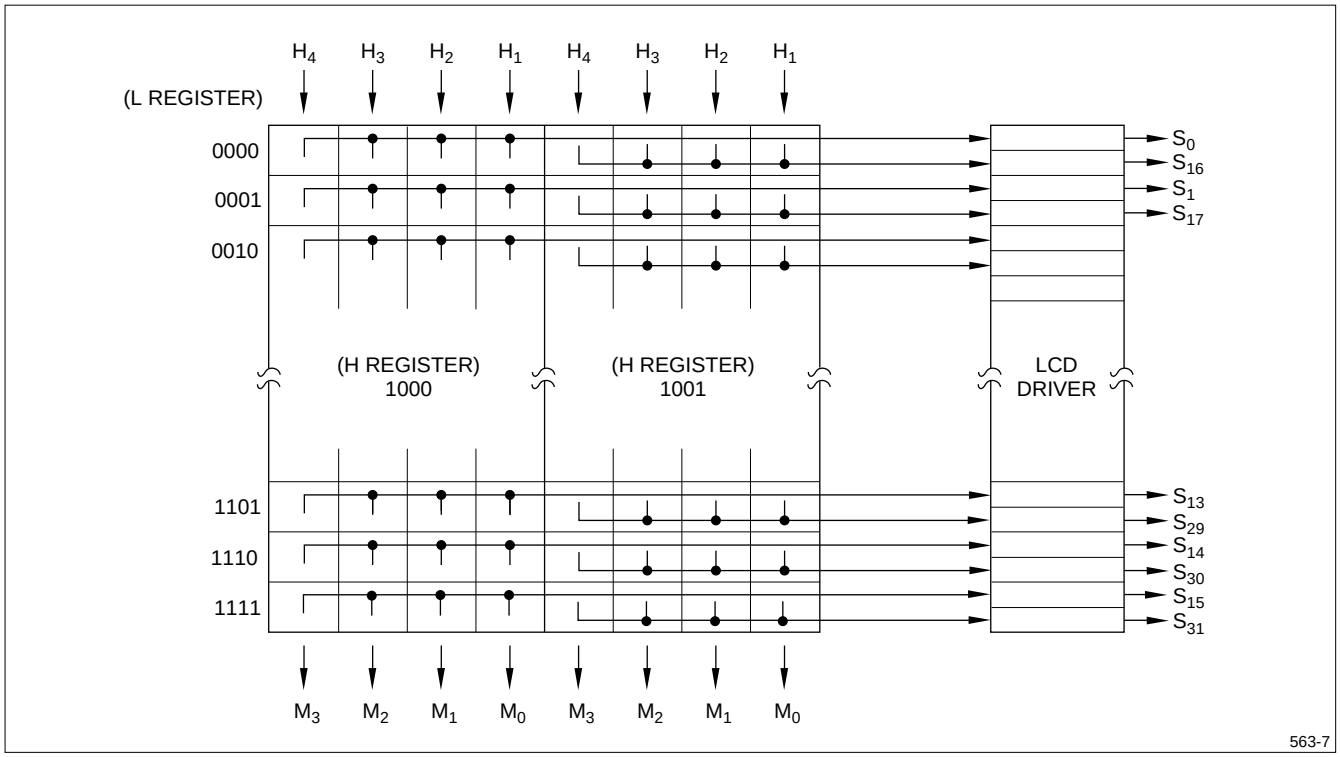


Figure 6. Display RAM and Its LCD Segment Outputs

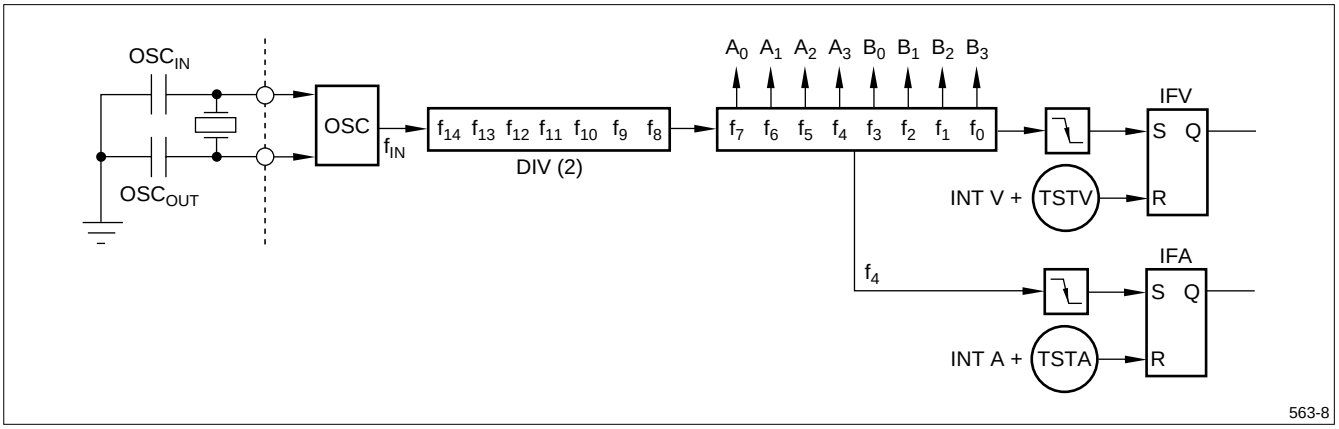


Figure 7. Real-Time Clock Divider

Accumulator (A), Subaccumulator (B) and Arithmetic and Logic Unit (ALU)

The accumulator (A) is a 4-bit working register which is the nucleus of the single chip system. It holds the results of operations and transfers data to memory, I/O ports and registers.

A subaccumulator (B) is another 4-bit register. It is used as one of the general purpose registers, and when combined with the A to form a B-A register pair, allows data transfer on an 8-bit basis.

The arithmetic and logic unit (ALU) performs, in conjunction with a carry flag (C), binary addition, shift operations and logical operations such as AND, OR, EX-OR and complement.

General Purpose Registers (H, L, D, E)

Registers H and L are 4-bit general purpose registers. They can transfer and compare data with the A on a 4-bit basis. Registers D and E are 4-bit registers and can transfer data with the H and L registers on an 8-bit basis. The H and L as well as the D and E registers can be combined into 8-bit register pairs, and can be used as pointers to data memory locations. The L register can be incremented or decremented and is used to access I/O ports and mode registers.

Clock Divider, IFV Flag, IFA Flag

The device contains a crystal oscillator and a 15-stage divider as shown in Figure 6. A real-time clock can be provided by connecting an external crystal oscillator between the oscillator pins. When an external 32.768 kHz crystal oscillator is used, the f_0 signal is a frequency of 1 Hz.

Timer/Counter and the SND Signal

The timer/counter consists of an 8-bit count register (TC) and an 8-bit modulo register (TM).

The count register is an 8-bit incremental binary counter. It is incremented by one at the falling edge of its count pulse (CP) input. If the count register overflows, the timer interrupt request flag IFT is set, and the contents of the modulo register (TM) are loaded into the count register (see Figure 7).

The count pulse Cp can be selected from divider signals f_{In}, f_8 and f_0, and the system clock, by using the mode register RD. If the count register (TC) overflows, the SND flag reverses its status at the falling edge of the TC. A sound signal can be obtained at the TC output by putting P2 in output mode and sending a '1' to pin $P2_3$ (see Figure 8).

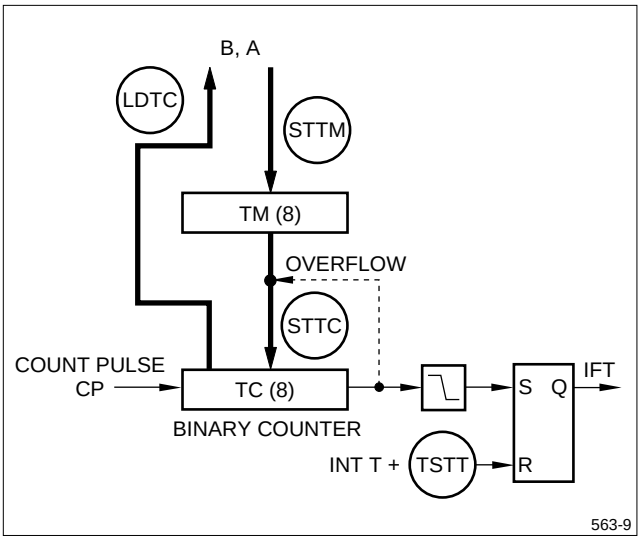


Figure 8. Timer/Counter

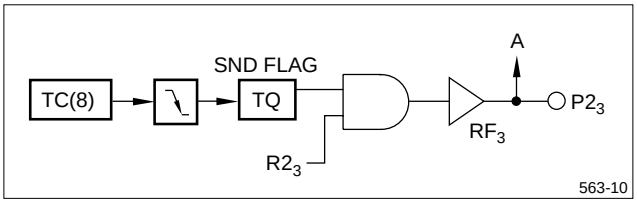


Figure 9. SND Signal

Serial Interface and IFS

The serial interface consists of an 8-bit shift register (SB) and a 3-bit counter, which is used to input and output the serial data. The serial clock can be selected with either an internal clock (system clock) or an external clock.

In serial shift operations, the highest bit data of the shift register (SB) is output from the SO pin, and the data input from the SI pin at the rising edge of a serial clock is loaded into the lowest bit of the shift register. When the internal clock is used, immediately after the SIO instruction is executed, the serial operation begins and stops with eight clocks which are output from the SCK pin.

Upon completion of an 8-bit shift operation, the serial I/O ending flag IFS is set each time a 3-bit counter overflows, and an interrupt request occurs.

Input Port P0 and IFB Flag

The IFB flag is set at the falling edge of the signal applied to the input port P0 by which the interrupt is enabled.

When port P0 is used as a key input, it can cause an interrupt each time a key is operated.

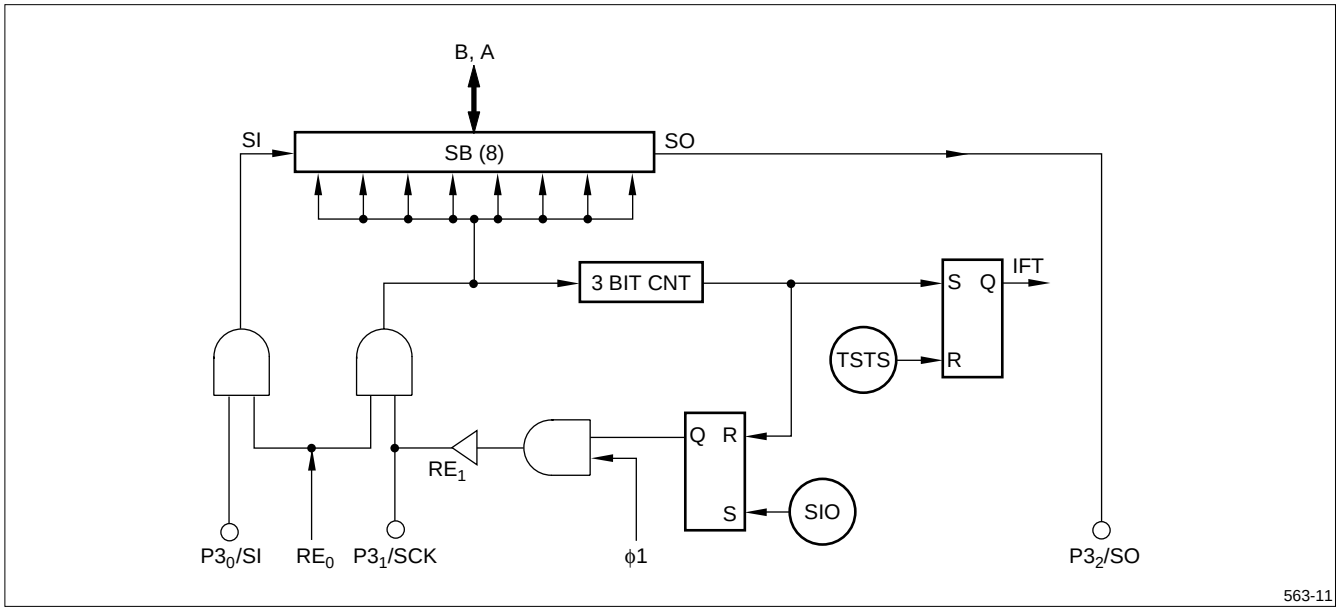


Figure 10. Serial Interface

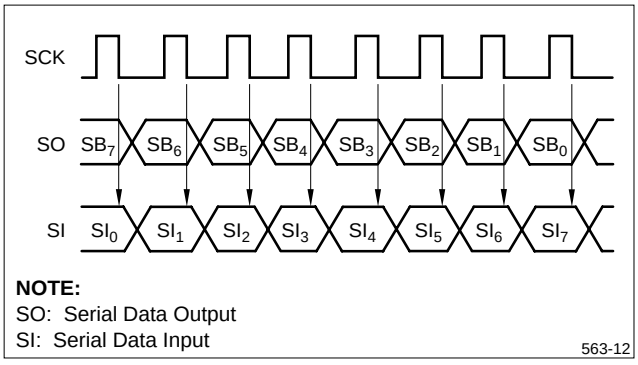


Figure 11. Serial Interface Timing

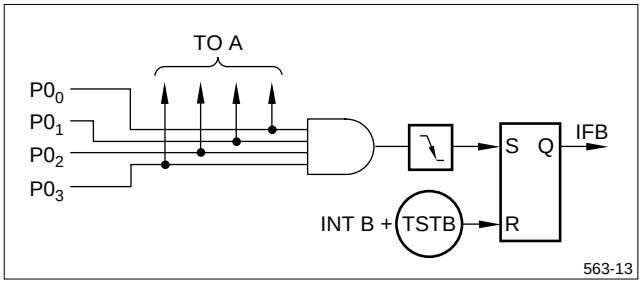


Figure 12. P0 Port

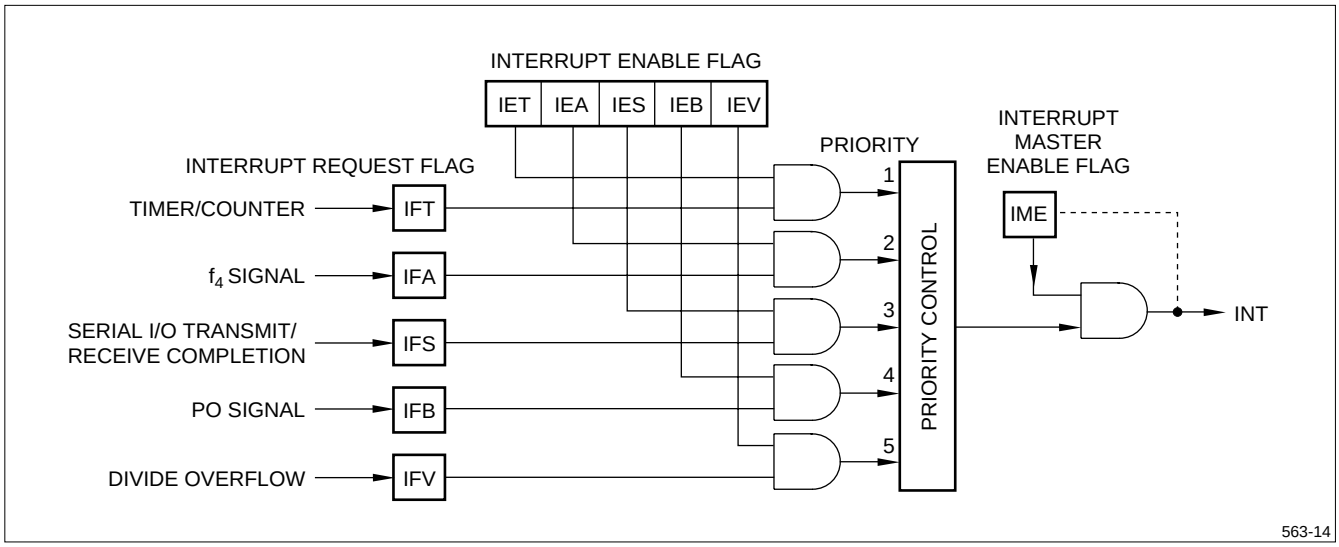


Figure 13. Interrupt Handling

Table 1. Characteristics of I/O Ports

PORT	FUNCTION	DIRECT 4-BIT PARALLEL I/O		IN, OUT INSTRUCTION		BIT INDEPENDENT OUTPUT SPN
		INPUT (INA)	OUTPUT (OUTA)	INPUT (IN)	OUTPUT (OUT)	DIRECT PIN-INDEPENDENT OUTPUT RPn
P0	Input-only port	O	X	O	X	X
P1	I/O port	O	O	X	O	O
P2	I/O port, $P2_3$ sound output	O	O	X	X	O
P3	$P3_0$ - SI, $P3_1$ - SCK, $P3_2$ - SO, multi-control port	O	O	X	X	O

NOTE: O - Yes, X - No

Interrupts

When an interrupt occurs, the corresponding interrupt request flag is set. The CPU acknowledges the interrupt if it is enabled (master interrupt enable flag and the corresponding interrupt enable flag are set). If more than one interrupt occurs simultaneously, all of the corresponding interrupt request flags will be set, but the CPU will only acknowledge that interrupt with the highest priority and other interrupts will be queued

I/O Ports

Port P0 is a 4-bit parallel input port. The IFB flag is set at the falling edge of this port.

Port P1 can be switched between input and output modes, 4-bits at a time.

Each bit of port P2 can be independently placed in input or output mode by setting the corresponding bit of mode register RF.

Ports $P2_0$ and $P2_1$ can output the OD and R/W signals, respectively. In those cases, these pins should be kept HIGH in an output mode. Port $P2_3$ outputs the SND signal in the output mode.

Port P3 is a 4-bit I/O port which can be placed in input or output mode, 3-bits at a time. Each bit of port P3 can be set the I/O modes (SI, SO, SCK) of a serial interface.

Ports P1 and P3 are placed in an output mode when a port output instruction is executed, and in an input mode when a port input instruction is executed. After an ACL operation, ports P1, P2 and P3 are all placed in an input mode.

Every input port has pull-up resistors. (Pull-up resistors for I/O ports are effective only when the ports are placed in an input mode.)

Ports P1 through P3 in an output mode can be independently set or reset by instructions.

When a key-matrix is configured by using I/O ports, a multiple key depression may cause a short to occur. To prevent this from occuring, port P1 should be used an an output.

Standby Mode

Executing the CEND instruction places the device in standby mode. To reduce power consumption, the system clock is inactivated. Standby mode may be cleared with the interrupt request or the $\overline{\text{RESET}}$ signal.

Reset Function (ACL)

Applying a LOW level signal to the $\overline{\text{RESET}}$ pin resets the internal logic of the device and applying a HIGH level signal starts execution of the program at address 0, page 0. Once the device is reset, all I/O ports are placed in input mode, all interrupts are disabled, and the LCD display turns off. The device is also reset when it is powered up.

Main Clock Oscillation Circuit

The main clock oscillator requires an external resistor across pins CK_1 and CK_2. Instead of using on-chip oscillator, an external clock may be applied to pin CK_1. In this case, pin CK_2 should be left open. The system clock ϕ is a divided clock equivalent to 1/4 of the clock applied to pin CK_1.

LCD Driver

Display Segment

The SM563 contains an on-chip LCD driver which can directly drive a LCD with a 1/4 duty and 1/3 bias. Figure 14 shows an example of LCD segment configuration for 1/4 duty.

Each segment of the LCD can be turned on or off by software control of the setting of the corresponding bit '1' or '0' in the display RAM area (see Figure 4).

The LCD digit may have any shape, provided that the maximum number of segments does not exceed 128 (see Figure 15). Figure 14 shows an example of a 7-segment numeric LCD digit.

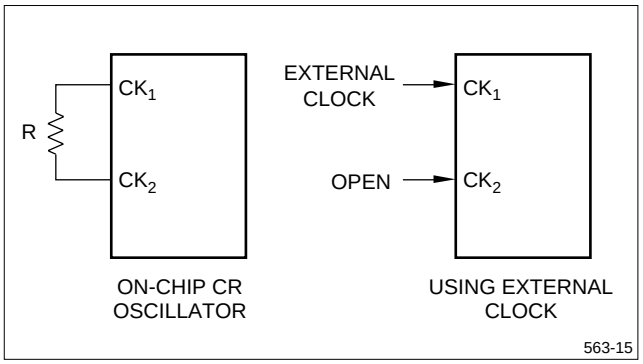


Figure 14. Main Clock Sources

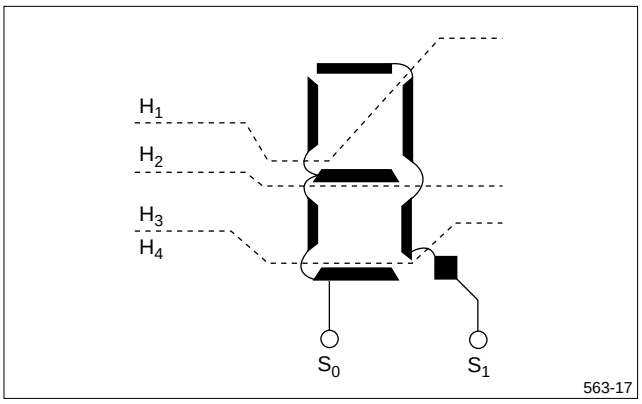


Figure 15. 7-Segment Numeric LCD Digit

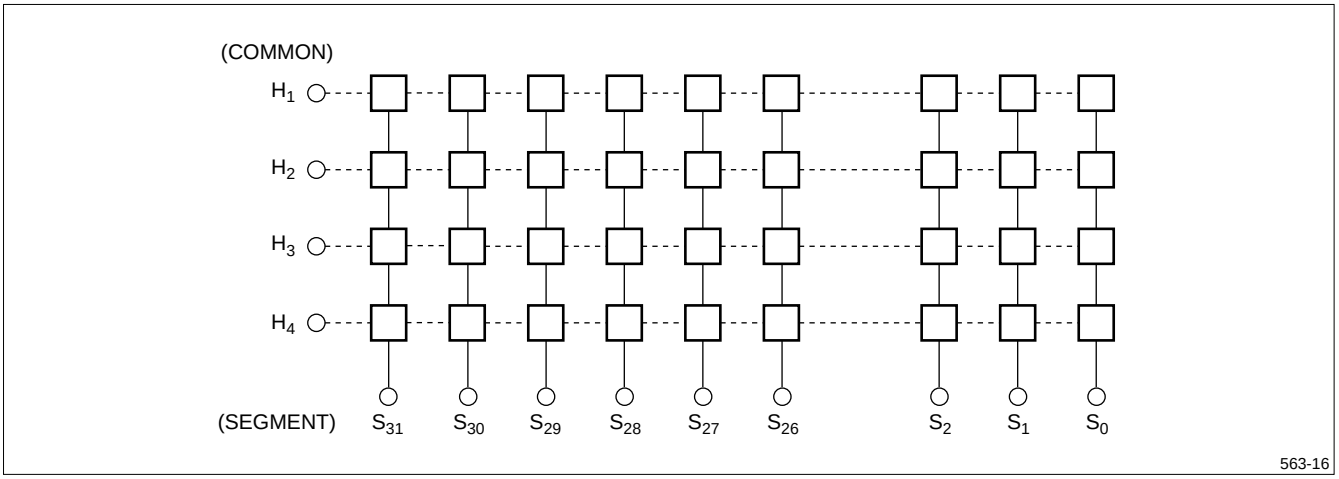


Figure 16. LCD Segment Configuration for 1/4 Duty

LCD Driving Signal Waveform

Figure 16 shows the LCD signal driving waveforms required to display the number '5' on the 7-segment display shown in Figure 14 (segment outputs S_0 and S_1 are used). A voltage of 3 V is applied to pin V_{DSP} in Figure 16. The frame frequency (I/T) can be selected from 64 Hz or 128 Hz by mask options.

V_{OA} and V_{OB}

The device contains bleeder resistors to allow 1/3 bias driving. When V_{DSP} is 3 V, voltages of 2 V and 1 V are output from pins V_{OA} and V_{OB} respectively. Normally pins V_{OA} and V_{OB} are left open. When an LCD with a large display area is driven, connect capacitors across pins V_{OA} and V_{DSP}, and across V_{OB} and V_{DSP} to improve the rise time of the LCD driving signal.

INSTRUCTION SET

ROM Address Instructions

MNEMONIC	MACHINE CODE	OPERATIONS
TR x	80 - BF	$P_L \leftarrow x\ (I_5 - I_0)$
TL xy (2-byte)	E0 - EF 00 - FF	$P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
TRS x	C0 - DF	(SP – 2), (SP – 3), (SP – 4) ← PC SP ← SP – 4 $P_U \leftarrow 10_H$ $P_L \leftarrow x\ (I_4, I_3, I_2, I_1, I_0, O)$
CALL xy (2-byte)	F0 - FF 00 - FF	(SP – 2), (SP – 3), (SP – 4) ← PC SP ← SP – 4, $P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
JBA x (2-byte)	7F 30 - 3F	$P_{U5}, - P_{U2} \leftarrow x\ (I_3 - I_0)$ $P_{U1}, P_{U0}, P_{L5}, P_{L4} \leftarrow B$ $P_{L3} - P_{L0} \leftarrow A$
RTN	61	$P_U, P_L \leftarrow$ (SP), (SP + 1), (SP + 2)
RTNS	62	$P_U, P_L \leftarrow$ (SP), (SP + 1), (SP + 2), SP ← SP + 4
RTNI	63	$P_U, P_L \leftarrow$ (SP), (SP + 1), (SP + 2), PSW ← (SP + 3), SP ← SP + 4 IME ← 1

RAM Address Instructions

MNEMONIC	MACHINE CODE	OPERATIONS
STL	69	L ← A
STH	68	H ← A
EXHD	3F	H ↔ D, L ↔ E
LIHL xy (2-byte)	3D 00 - FF	H ← $(I_7 - I_4)$, L ← y $(I_3 - I_0)$

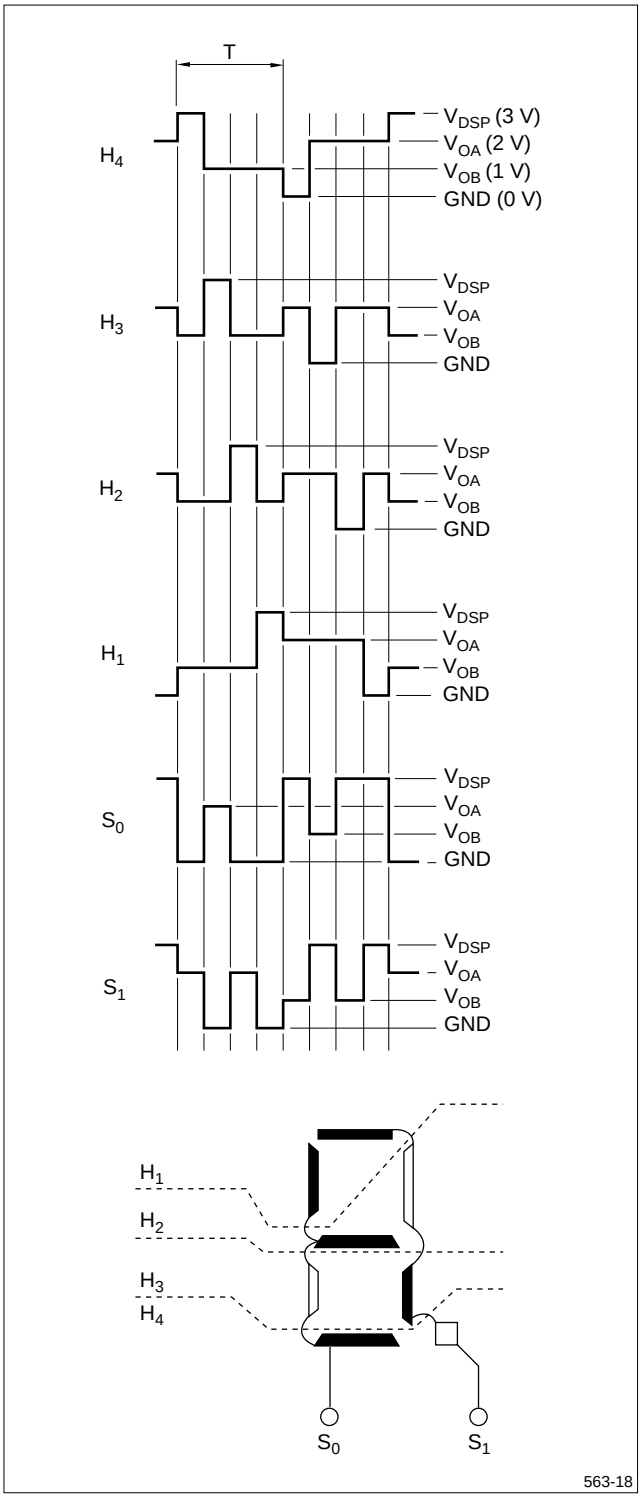


Figure 17. LCD Driving Signal Waveform (Required to Display the Number 5)

Data Transfer Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
EX pr	5C - 5F	A ↔ (pr)
LDX adr (2-byte)	7D 00 - FF	A ← (adr)
STX adr (2-byte)	7E 00 - FF	(adr) ← A
EXX adr (2-byte)	7C 00 - FF	A ↔ (adr)
LAX x	10 - 1F	A ← x (I_3 – I_0)
LIBA xy (2-byte)	3C 00 - FF	B ← x (I_7 – I_4) A ← y (I_3 – I_0)
LBAT	60	B ← ROM (P_{U5} – P_{U2}, B, A)$_H$ A ← ROM (P_{U5} – P_{U2}, B, A)$_L$
LDL	65	A ← L
LD pr	54 - 57	A ← (pr)
ST pr	58 - 5B	(pr) ← A
EXH	6C	A ↔ H
EXL	6D	A ↔ L
EXB	6E	A ↔ B
STB	6A	B ← A
LDB	66	A ← B
LDH	64	A ← H
PSHBA	28	(SP – 1) ← B, (SP ← 2) ← A, SP ← SP – 2
PSHHL	29	(SP – 1) ← H, (SP ← 2) ← L, SP ← SP –2
POPBA	38	B ← (SP + 1), A ← (SP), SP ← SP + 2
POPHL	39	H ← (SP + 1), L ← (SP), SP ← SP + 2
STSB	70	SB_H ← B, SB_L ← A
STSP	71	SP_H ← B, SP_L ← A
STTC	72	TC ← TM
STTM	73	TM_H ← B, TM_L ← A
LDSB	74	B ← SB_H, A ← SB_L
LDSP	75	B ← SP_H, A ← SP_L
LDTC	76	B ← TC_H, A ← TC_L
LDDIV	77	B ← DIV_H, A ← DIV_L

Arithmetic Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
ADX x	00 - 0F	A ← A + x (I_3 – I_0), Skip if C_Y = 1
ADD	36	A ← A + (HL)
ADDC	37	A ← A + (HL) + C, C ← C_Y Skip if C_Y = 1
OR	31	A ← A ∪ (HL)
AND	32	A ← A ∩ (HL)
EOR	33	A ← A ⊕ (HL)
ANDB	22	A ← A ∩ B
ORB	21	A ← A ∪ B
EORB	23	A ← A ⊕ B
COMA	6F	A ← $\overline{A}$
ROTR	25	C → A_3 → A_2 → A_1 → A_0 → C
ROTL	35	C ← A_3 ← A_2 ← A_1 ← A_0 ← C
INCB	52	B ← B + 1, Skip if B = F_H
DECB	53	B ← B – 1, Skip if B = 0
INCL	50	L ← L + 1,Skip if L = F_H
DECL	51	L ← L – 1, Skip if L = 0
DECM adr	79 00 - FF	(adr) ← (adr) – 1, Skip if (adr) = 0
INCM adr	78 00 - FF	(adr) ← (adr) + 1, Skip if (adr) = F_H

Test Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TAM	30	Skip if A = (HL)
TAH	24	Skip if A = H
TAL	34	Skip if A = L
TAB	20	Skip if A = B
TC	2A	Skip if C = 0
TM x	48 - 4B	Skip if (HL)x = 1
TA x	4C - 4F	Skip if Ax = 1
TSTT	2B	Skip if IFT = 1, IFT ← 0
TSTA	2C	Skip if IFA = 1, IFA ← 0
TSTS	2D	Skip is IFS = 1, IFS ← 0
TSTB	2E	Skip if IFB = 1, IFB ← 0
TSTV	2F	Skip if IFV = 1, IFV ← 0

Bit Manipulation Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
SM x	40 - 43	(HL)x ← 1
RM x	44 - 47	(HL)x ← 0
RC	26	C ← 0
SC	27	C ← 1
RIME	3A	IME ← 0
SIME	3B	IME ← 1
DI x (2-byte)	7F C0 - DF	IEF ← IEF ∩ x
EI x (2-byte)	7F E0 - FF	IEF ∪ x

Special Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
SIO	3E	Serial I/O start
IDIV (2-byte)	7F 10	DIV ← 0
SKIP	00	No operation
CEND (2-byte)	7F 00	System clock stop

NOTE: The machine code consists of 8-bits including I_7, I_6, I_5, I_4, I_3, I_2, I_1 and I_0

I/O Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
IN	67	A ← P0
OUT	6B	P1 ← A
INA x (2-byte)	7F A0 - A9	A ← P (x), R (x)
OUTA (2-byte)	7F B0 - BF	P (x), R (x) ← A
INBA x	7F 80 - 82	B ← R (x + 1) A ← R (x)
OUTBA x (2-byte)	7F 90 - 93	R (x + 1) ← B R (x) ← A
SP xy (2-byte)	7A 00 - F3	P (y) ← P (y) x
BP xy (2-byte)	7B 00 - F3	P (y) ← P (y) x
RDS (2-byte)	7F 60	DS ← 0
RBR (2-byte)	7F 70	BR ← 0
SDS (2-byte)	7F 61	DS ← 1
SBR (2-byte)	7F 71	BR ← 0
READ (2-byte0	7F 62	A ← P4 with OD
WRIT (2-byte)	7F 72	P4 ← A with R/W
READB (2-byte)	7F 63	A ← P4, with OD B ← P5
WRITB (2-byte)	7F 73	P4 ← A, with R/W P5 ← B

SYSTEM CONFIGURATION EXAMPLE

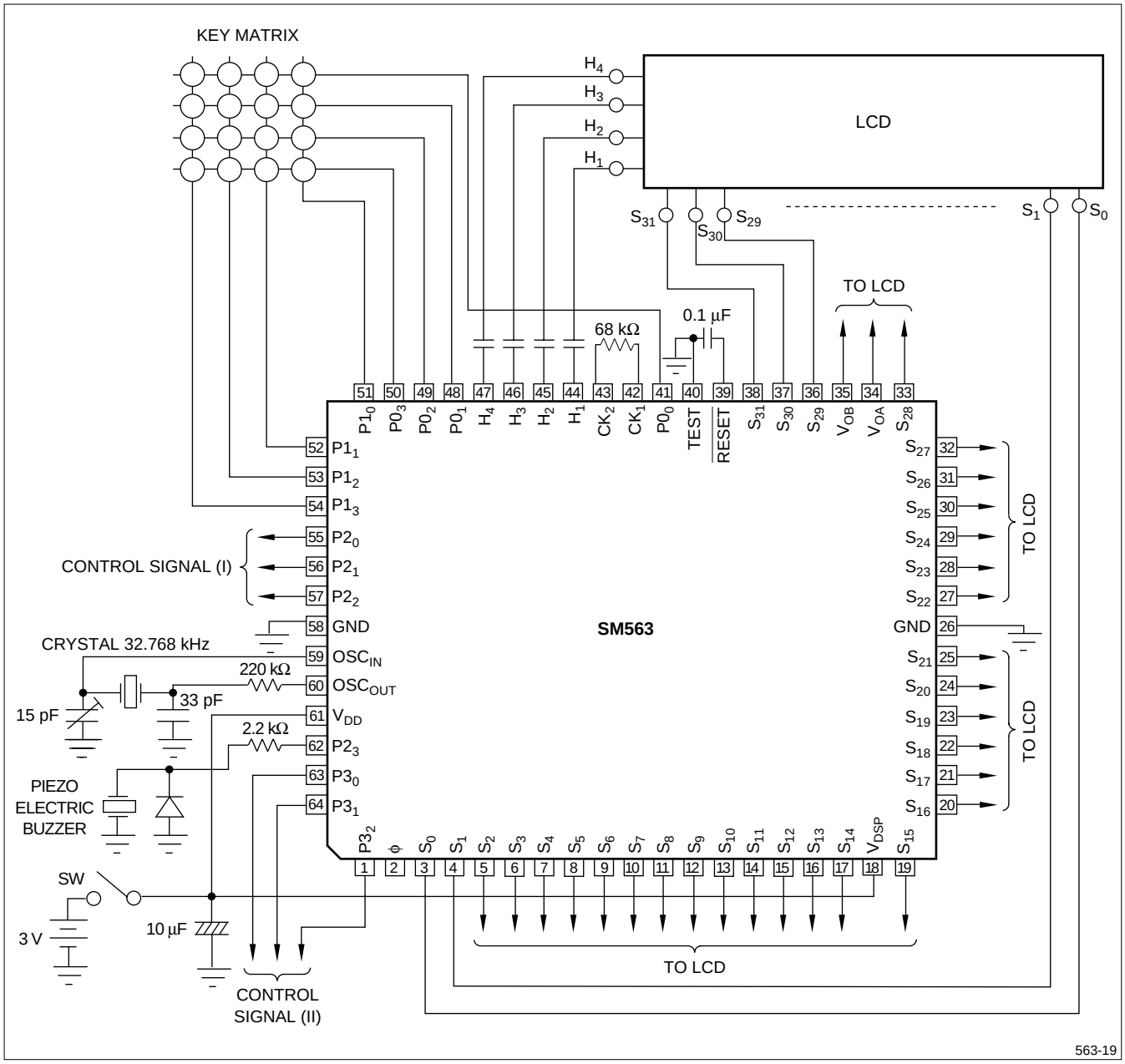


Figure 18. Example of a Home Security System

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