SM5K6/SM5K7
4-Bit Single-Chip Microcomputer

FEATURES

- ROM Capacity
  - 4,096 × 8-bits (SM5K6)
  - 8,192 × 8-bits (SM5K7)
- RAM Capacity
  - 256 × 4-bits (SM5K6)
  - 512 × 4-bits (SM5K7)
- Instruction Sets
  - 52 Sets (SM5K6)
  - 54 Sets (SM5K7)
- 8 Levels of Subroutine Nesting
- Input/Output Ports
  - 4 Input Ports
  - 20 Input/Output Ports
- Interrupts
  - Internal Interrupt × 3 (2 Timers, 1 Serial Interface)
  - External Interrupt × 2 (2 External Interrupt Inputs)
- A/D Converter
  - 10-bits Resolution
  - 8 Channels
- Timer/Counter 8-bit × 2
- Serial Interface 8-bit Synchronous × 1
- Watchdog Timer 8-bit × 1 (Also Used as Timer 2)
- Built-in Main Clock Oscillator for System Clock
  - CR/Ceramic/Crystal Oscillator
- Signal Generation for Real Time Clock[1]
- Built-in 15 Stages Divider for Real Time Clock[1]
- Instruction Cycle Time
  - 1 µs (MIN.), 4 MHz, at 5 V ±10%
  - 4 µs (MIN.), 1 MHz at 2.0 V to 5.5 V
  - 122 µs (MAX.), 32.768 kHz at 2.0 V to 5.5 V
- Large Current Output Pins (LED Direct Drive)
  - 15 mA (TYP.) × 8 (Sink Current)
- Buzzer Output
- Supply Voltages 2.20 V to 5.5 V
- Packages
  - 30-pin SDIP (SDIP030-P-400)[2]
  - 32-pin SOP (SOP032-P-0525)[3]
  - 36-pin QFP (QFP036-P-1010)[3]

NOTES:
1. When using the crystal oscillator.
2. OTP microcomputer is available for SM5K6.
3. OTP microcomputer is available for SM5K6/SM5K7.

DESCRIPTION

The SM5K6/5K7 are CMOS 4-bit single-chip microcomputers incorporating 4-bit parallel processing function, serial interface function, ROM, RAM, 10-bit A/D converter and timer/counters. It provides five kinds of interrupts and 8 levels subroutine stack. Being fabricated through CMOS process, the chip requires less power and is available in a small package. Best suited for low power controlling, compact equipment like a precision charger.

PIN CONNECTIONS

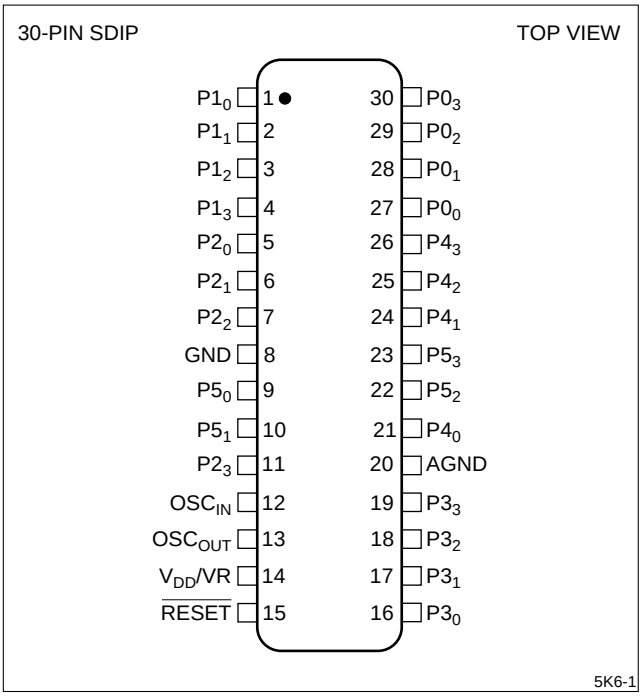


Figure 1. 30-Pin SDIP

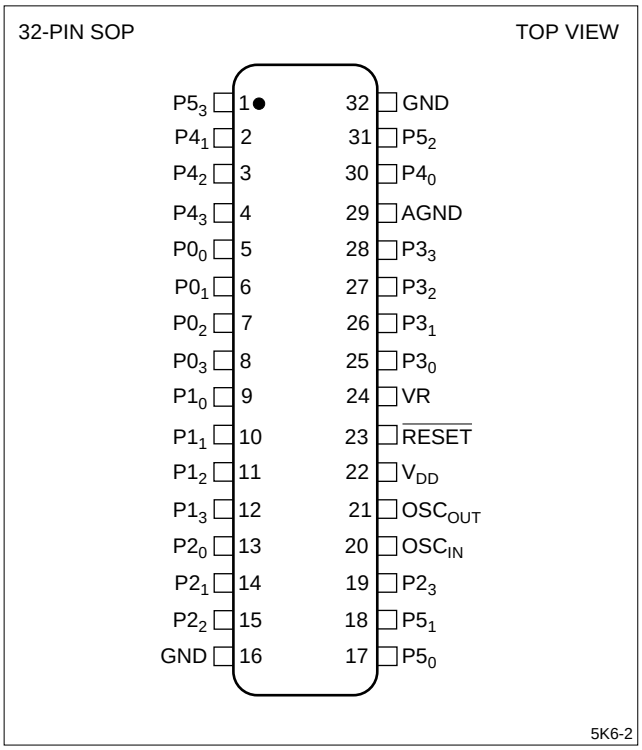


Figure 2. 32-Pin SOP

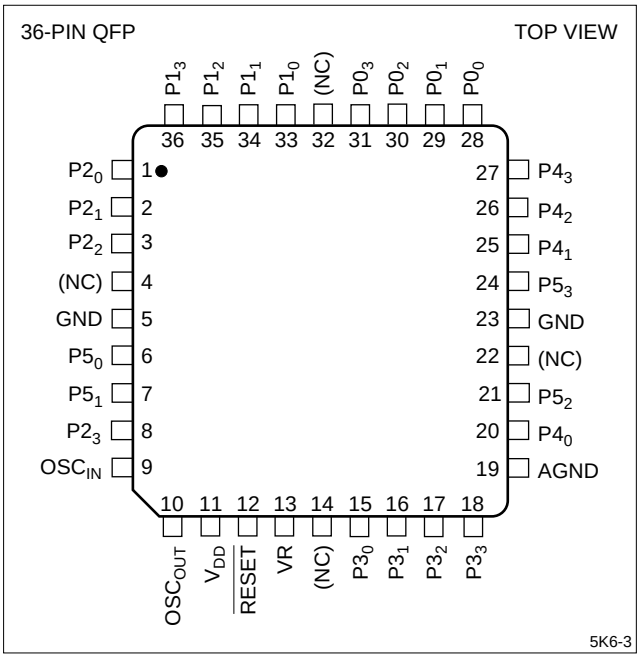
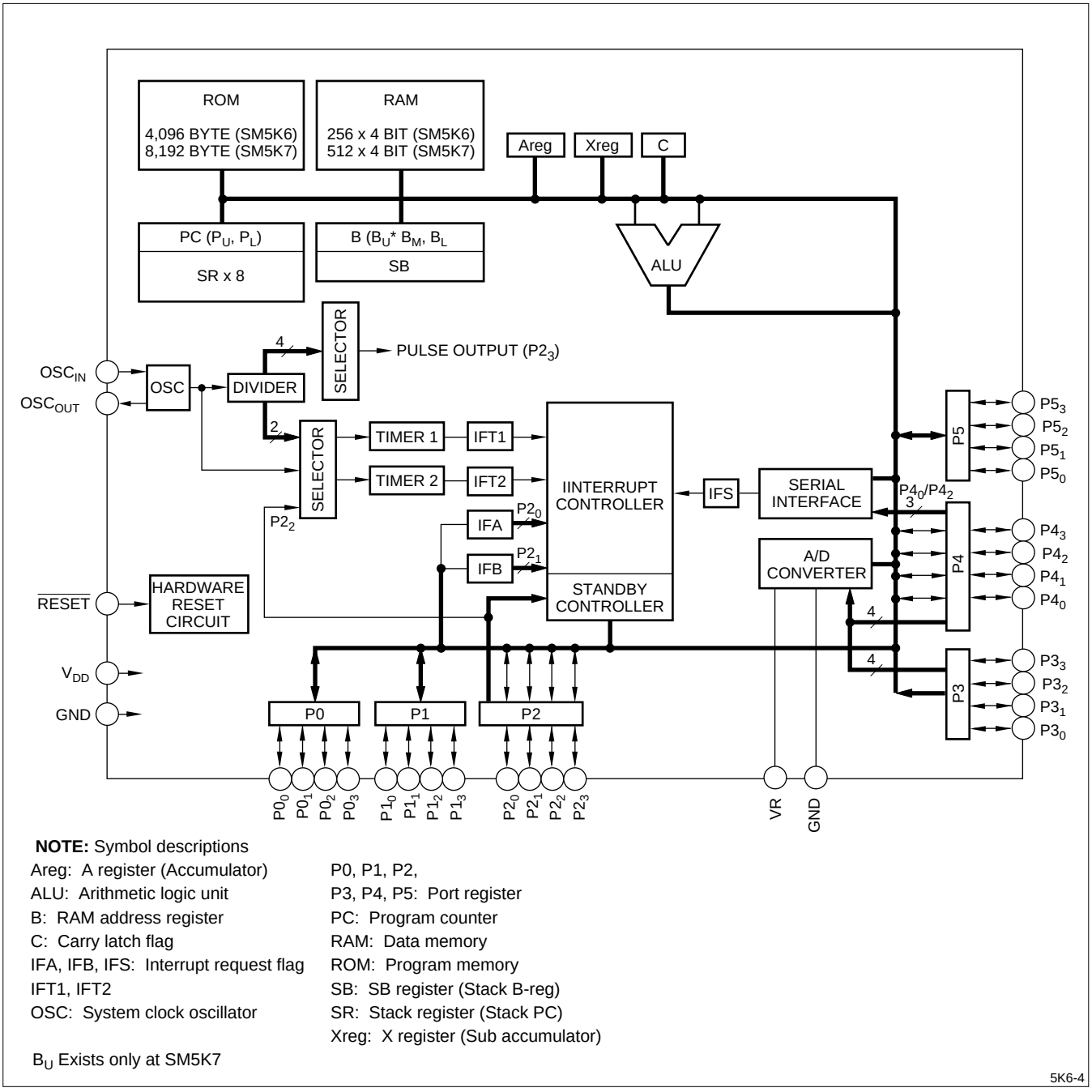


Figure 3. 36-Pin QFP



NOTE: Symbol descriptions

Areg: A register (Accumulator)
ALU: Arithmetic logic unit
B: RAM address register
C: Carry latch flag
IFA, IFB, IFS: Interrupt request flag
IFT1, IFT2
OSC: System clock oscillator

P0, P1, P2,
P3, P4, P5: Port register
PC: Program counter
RAM: Data memory
ROM: Program memory
SB: SB register (Stack B-reg)
SR: Stack register (Stack PC)
Xreg: X register (Sub accumulator)

B_U Exists only at SM5K7

Figure 4. Block Diagram

PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
$P0_0$ - $P0_3$, $P1_0$ - $P1_1$	I/O	Input/Output, direction of pins can be set in units of 4-bits. When set at output, each pin serves as a drive with a 15 mA (TYP.) current sinking capability.
$P2_0$ - $P2_2$	I/O	Input or output (independent), direction of this pin can be set independently. Assumes external interrupt input or standby release.
$P2_3$	I/O	Input or output (independent), direction of this pin can be set independently. Assumes standby release or buzzer output (divider clock).
$P3_0$ - $P3_3$	I	Input, accepts input in units of 4-bits. Also assumes A/D pins.
$P4_0$, $P4_1$	I/O	Input or output (independent), direction of this pin can be set independently. Assumes A/D pin or SIO data output.
$P4_2$	I/O	Input or output (independent), direction of this pin can be set independently. Assumes A/D pin or SIO clock I/O.
$P4_3$	I/O	Input or output (independent), direction of this pin can be set independently. Also assumes A/D pin.
$P5_0$ - $P5_3$	I/O	Input/output, direction of pins can be set in units of 4-bits.
$\overline{\text{RESET}}$	I	Hardware reset input, input to this pin resets the microcomputer. For normal run, connect 0.1 µF (TYP.) across $\overline{\text{RESET}}$ and GND pins.
OSC_{IN}, OSC_{OUT}	I, O	Main clock circuit pins. Connecting a crystal across these pins completes main clock oscillator. The divided-by-4 main clock is used as the system clock
V_{DD}, GND		Power supply input to the microcomputer.
VR, GND		A/D converter reference voltage, connect to VR to V_{DD} pin and AGND to GND pin.

NOTES:
1. Hardware reset sets all I/O pins to input.
2. Input ports and I/O ports programmed as input port are provided with pull-up resistors.

ABSOLUTE MAXIMUM RATINGS

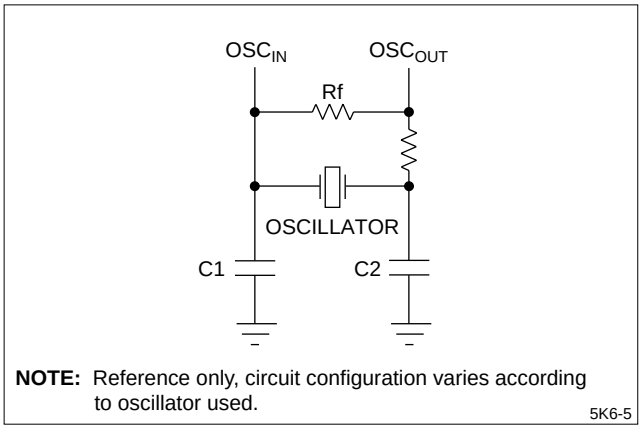
PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		-0.3 to +7.0	V
Input voltage	V_{IN}		-0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		-0.3 to V_{DD} + 0.3	V
Maximum output current	I_{OH}	HIGH level output current (at each output)	4	mA
	I_{OL0}	LOW level output current ($P0_0$ - $P0_3$, $P1_0$ - $P1_3$)	30	mA
	I_{OL1}	LOW level output current (all but $P0_0$ - $P0_3$, $P1_0$ - $P1_3$)	4	mA
Total output current	ΣI_{OH}	HIGH level output current (all outputs)	20	mA
	ΣI_{OL}	LOW level output current (all outputs)	120	mA
Operating temperature	T_{OPR}		-20 to +70	°C
Storage temperature	T_{STG}		-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	V_{DD}		2.0 to 5.5	V
Instruction cycle	t_{CYC}	V_{DD} = 2.0 V to 5.5 V	4 to 122	µs
		V_{DD} = 5.0 V ±10%	1 to 122	µs
System clock frequency	f_{SYS}	V_{DD} = 2.0 V to 5.5 V	250 k to 8.192 k	Hz
		V_{DD} = 5.0 V ±10%	1 M to 8.192 k	Hz
Main clock frequency (OSC_{IN}, OSC_{OUT})	f_{OSC}	V_{DD} = 2.0 V to 5.5 V	1 M to 32.768 k*	Hz
		V_{DD} = 5.0 V ±10%	4 M to 32.768 k*	Hz

NOTE: *A crystal oscillator is used for the frequency 32.768 kHz only.

OSCILLATION CIRCUIT



NOTE: Reference only, circuit configuration varies according to oscillator used.

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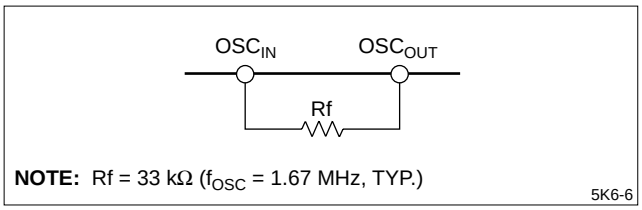
Figure 5. Ceramic/Crystal OSC



NOTE: Rf = 33 kΩ (f_{OSC} = 1.67 MHz, TYP.)

5K6-6

Figure 6. CR OSC

NOTES:

1. The typical oscillation frequency shall be determined in consideration of operating condition and fluctuation frequency.
2. Mount Rf, RD, C_1, C_2 Oscillator (Ceramic/Crystal OSC)/Rf (CR OSC) as close as possible to the oscillator pins of the LSI in order to reduce an influence from floating capacitance.
3. Since the value of resistor Rf, RD, C_1, C_2, Oscillator (Ceramic/Crystal OSC)/Rf (CR OSC) varies depending on circuit pattern and others, the final Rf, RD, C_1, C_2, Oscillator (Ceramic Crystal OSC)/Rf (CR OSC) value shall be determined on the actual unit.
4. Don't connect any line to OSC_{IN} and OSC_{OUT} except oscillator circuit.
5. Don't put any signal line across the oscillator circuit line.
6. On the multi-layer circuit, do not let oscillator circuit wiring cross other circuit.
7. Minimize the wiring capacitance of GND and V_{DD}.

DC CHARACTERISTICS

V_{DD} = 5.0 V or 3.0 V, T_{OPR} = -20°C to +70°C (TYP.) unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTES
Input voltage	V_{IH1}		0.8 × V_{DD}		V_{DD}	V	1
	V_{IL1}		0		0.2 × V_{DD}	V	1
	V_{IH2}		0.9 × V_{DD}		V_{DD}	V	2
	V_{IL2}		0		0.1 × V_{DD}	V	2
Input current	I_{IL1}	V_{IN} = 0 V, V_{DD} = 2.0 V to 3.3 V	2	25	90	µA	3
		V_{IN} = 0 V, V_{DD} = 4.5 V to 5.5 V	25	70	250	µA	3
	I_{IH1}	V_{IN} = V_{DD}			2	µA	3
	I_{IL2}	V_{IN} = 0 V		1	10	µA	4
	I_{IH2}	V_{IN} = V_{DD}		1	10	µA	4
Output current	I_{OL1}	V_O = 1.0 V, V_{DD} = 2.0 V to 3.3 V	3	15		mA	5
		V_O = 1.0 V, V_{DD} = 4.5 V to 5.5 V	15	25		mA	5
	I_{OH1}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.0 V to 3.3 V	0.2	1.5		mA	5
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	1	2.2		mA	5
	I_{OL2}	V_O = 0.5 V, V_{DD} = 2.0 V to 3.3 V	80	600		µA	6
		V_O = 0.5 V, V_{DD} = 4.5 V to 5.5 V	400	1,000		µA	6
	I_{OH2}	V_O = V_{DD} – 0.5 V, V_{DD} = 2.0 V to 3.3 V	250	2,000		µA	6
		V_O = V_{DD} – 0.5 V, V_{DD} = 4.5 V to 5.5 V	1,000	2,400		µA	6

NOTES:

1. Applicable pins; $P0_0$ - $P0_3$, $P1_0$ - $P1_3$, $P2_2$, $P2_3$, $P3_0$ - $P3_3$, $P4_1$, $P4_3$ (digital input mode), $P5_0$ - $P5_3$.
2. Applicable pins: OSC_{IN}, $\overline{RESET}$, $P2_0$, $P2_1$, $P4_0$, $P4_2$ (digital input mode).
3. Applicable pins: $P3_0$ - $P3_3$, $P4_0$ - $P4_3$, (digital input mode), $\overline{RESET}$, $P0_0$ - $P0_3$, $P1_0$ - $P1_3$, $P2_0$ - $P2_3$, $P5_0$ - $P5_3$.
4. Applicable pins: $P3_0$ - $P3_3$, $P4_0$ - $P4_3$ (A/D mode).
5. Applicable pins: $P0_0$ - $P0_3$, $P1_0$ - $P1_3$ (high current mode).
6. Applicable pins: $P2_0$ - $P2_3$, $P4_0$ - $P4_3$, $P5_0$ - $P5_3$ (output mode).

DC CHARACTERISTICS (Cont'd)

V_{DD} = 5.0 V or 3.0 V, T_{OPR} = -20°C to + 70°C (TYP.) unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.*	MAX.*	UNIT	NOTES
Supply current	I_{DD}	f_{OSC} = 2 MHz, V_{DD} = 4.5 V to 5.5 V		1,600/1,800	3,500/4,200	µA	7
		f_{OSC} = 1 MHz, V_{DD} = 2.0 V to 3.3 V		400/500	1,100/1,400	µA	7
		f_{OSC} = 1 MHz, V_{DD} = 4.5 V to 5.5 V		850/1,000	1,700/2,000	µA	7
		f_{OSC} = 40 kHz, V_{DD} = 2.0 V to 3.3 V		80/90	200/250	µA	7
		f_{OSC} = 40 kHz, V_{DD} = 4.5 V to 5.5 V		200/250	500/600	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.0 V to 3.3 V		28/35	170/220	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 4.5 V to 5.5 V		55/70	220/280	µA	7
	I_{HALT}	f_{OSC} = 2 MHz, V_{DD} = 4.5 V to 5.5 V		900/1,000	1,800/2,200	µA	7
		f_{OSC} = 1 MHz, V_{DD} = 4.5 V to 5.5 V		500/600	1,100/1,400	µA	7
		f_{OSC} = 40 kHz, V_{DD} = 2.0 V to 3.3 V		50/60	120/150	µA	7
		f_{OSC} = 40 kHz, V_{DD} = 4.5 V to 5.5 V		180/220	450/550	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.0 V to 3.3 V		20/25	75/90	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 4.5 V to 5.5 V		25/30	120/150	µA	7
	I_{STOP}	CR, Ceramic OSC mode, V_{DD} = 2.0 V to 5.5 V			3.0/3.0	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 2.0 V to 5.5 V		20/25	45/90	µA	7
		f_{OSC} = 32.768 kHz (crystal OSC mode) V_{DD} = 4.5 V to 5.5 V		25/35	65/70	µA	7
	I_{VR}	A/D in operation, V_{DD} = 2.0 V to 3.3 V		180	420	µA	8
		A/D in operation, V_{DD} = 4.5 V to 5.5 V		300	650	µA	8
		A/D in stop, V_{DD} = 2.0 V to 5.5 V			3.0	µA	9
A/D conversion	Resolution			10		bit	
	Differential linearity error	f_{OSC} = 2 MHz, T_{OPR} = 25°C, V_{DD} = VR = 5.0 V		±2.5	±4.0	LSB	
	Sequential linearity error			±3.2	±5.0	LSB	
	Total error			±4.0	±6.0	LSB	

NOTES:

7. No load (A/D conversion disabled).
8. Current into VR at A/D conversion mode (run enable status).
9. Current into VR at non-AD conversion mode (run disable status).
10. * SM5K6/SM5K7.

SYSTEM CONFIGURATION

A Register and X Register

The A register (or accumulator A_{CC}) is a 4-bit general purpose register. The register is mainly used in conjunction with the ALU, C flag and RAM to transfer numerical value and data to perform various operations. The A register is also used to transfer data between input and output pins.

The X register (or auxiliary accumulator) is a 4-bit register and can be used as a temporary register. It loads contents of the A register or its content is transferred to the A register.

When the table reference instruction PAT is used, the X and A registers load ROM data. A pair of A and X registers can accommodate 8-bit data.

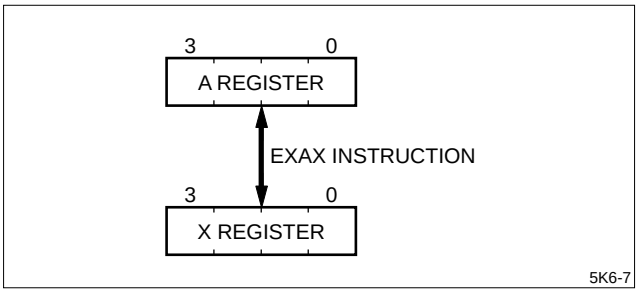


Figure 7. Data Transfer Example Between A Register and X Register

Arithmetic and Logic Unit (ALU) and Carry Signal Cy

The ALU performs 4-bit parallel operation. The ALU operates binary addition in conjunction with RAM, C flag and A register. Cy is the symbol for carry signal and not for C flag.

The C flag latches the carry-over as the result of arithmetic instruction. The flag can be set/cleared using SC and RC instructions. The content of C flag can be tested using the TC instruction.

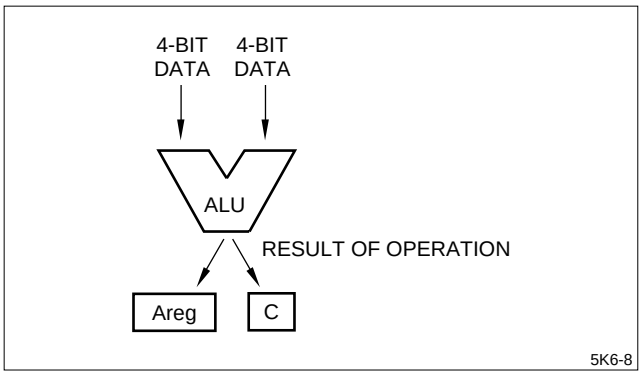


Figure 8. ALU

B Register and SB Register

B Register (B_U (SM5K7 only), B_M, B_L)

The B register is an 8-bit/9-bit register that is used to specify the RAM address. The upper 4-bit section is called B_M register and lower 4-bit B_L.

SB Register (B_U (SM5K7 only), B_M, B_L)

The SB register is an 8-bit/9-bit register used as the save register for the B register. The contents of B register and SB register can be exchanged through EX instruction.

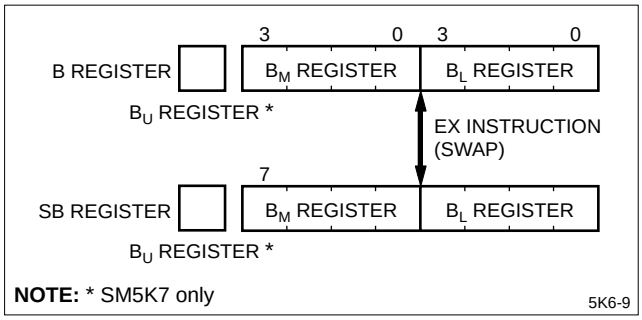


Figure 9. B Register and SB Register

Data Memory (RAM)

The data memory (RAM) is used to store data up to 256 × 4-bits (256 nibbles) (SM5K6), and 512 × 4-bits (512 nibbles) (SM5K7).

Program Counter PC and Stack Register SR

Program Counter PC and Stack (SR)

The program counter consists of a 6-bit/7-bit page address register (P_U) and 6-bit binary counter (P_L) used to specify the steps within a page. The stack pointer (SP) is a register which holds the starting address of the stack area of RAM space.

Precaution on Using PAT Instruction

Execution of interrupt handling or the table reference instruction PAT automatically uses one level of the stack register SR, as in the case of subroutine handing process.

B_U	0																1															
B_M / B_L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																																
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E																																
F																																*

NOTES:

1. * 1 nibble = 4-Bit
2. SM5K6 uses areas of B_U = 0
3. SM5K7 use whole area

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Figure 10. RAM Map

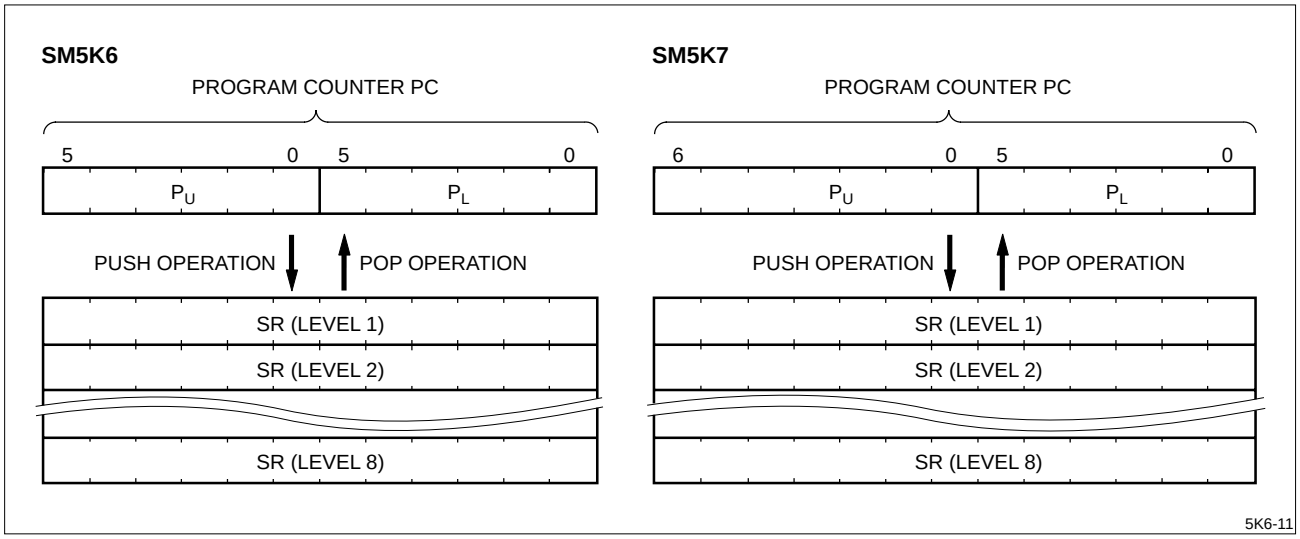

Figure 11. Program Counter PC and Stack Register SR

Program Memory (ROM)

The ROM is used to store the user program. The capacity of the ROM is 4,096 bytes (64 page by 64-byte) (SM5K6), 8,192 bytes (128 page by 64-byte) SM5K7.

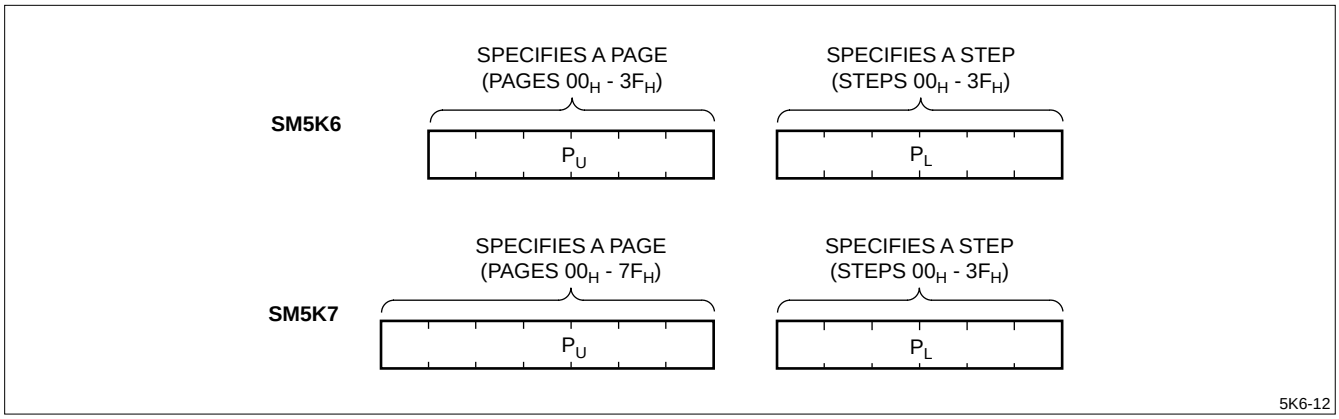

Figure 12. Page and Step for ROM

P_{U6}	0				1			
P_{U4-5} / P_{U0-3}	0	1	2	3	0	1	2	3
0	①							
1	②							
2	③							
3	④							
4								
5								
6								
7								
8								
9								
A								
B								
C								
D								
E								
F				⑤				⑥

NOTES:
1. SM5K6 uses areas of $PU_6 = 0$
2. SM5K7 use whole area

① Start address upon reset (0000_H)
② Front cover of subroutine TRS
③ Interrupt
④ Standby release
⑤ Final address (SM5K6)
⑥ Final address (SM5K7)

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Figure 13. ROM Configuration

Control Registers

Most of the SM5K6/5K7 functions are controlled by reading and writing 22 control registers.

Table 1. Control Registers

ADDRESS		SYMBOL	NAME	UNIT	AVAILABLE INSTRUCTIONS				
B_M	B_L				INTL	OUTL	IN/TPB	OUT	ANP/ORP
*	0	P0	P0 port	4	—	—	O	—	—
			P0 register	4	—	O	—	O	O
*	1	P1	P1 port	4	—	—	O	—	—
			P1 register	4	—	O	—	O	O
*	2	P2	P2 port	4	—	—	O	—	—
			P2 register	4	—	—	—	O	O
*	3	P3	P3 port	4	O	—	O	—	—
		R3	P3 mode register	4	—	—	—	O	O
*	4	P4	P4 port	4	—	—	O	—	—
			P4 register	4	—	—	—	O	O
*	5	P5	P5 port	4	—	—	O	—	—
			P5 register	4	—	—	—	O	O
*	6	R6	P4 direction register	4	—	—	O	O	O
*	7	R7	A/D select register	4	—	—	O	O	O
0	8	R08	A/D control register	8	—	—	Δ	O	—
0	9	R09	A/D data register	8	—	—	Δ	O	—
0	A	R0A	Timer 1 counter	8	—	—	Δ	Δ	—
0	B	R0B	Timer 1 modulo register	8	—	—	Δ	O	—
0	C	R0C	Timer 1 control register	4	—	—	O	O	O
*	D	RD	P4 mode register	4	—	—	O	O	O
*	E	RE	Interrupt enable register	4	—	—	O	O	O
0	F	R0F	P2 direction register	4	—	—	O	O	O
1	8	R18	SIO shift register	8	—	—	Δ	O	—
1	9	R19	SIO control register	8	—	—	Δ	O	—
1	A	R1A	Timer 2 counter	8	—	—	Δ	Δ	—
1	B	R1B	Timer 2 modulo register	8	—	—	Δ	O	—
1	C	R1C	Timer 2 control register	4	—	—	O	O	O
1	F	R1F	Buzzer control register	4	—	—	O	O	O

NOTES:
1. *Don't care.
2. O = Executable
   Δ = Executable but with some restriction
   — = Not executable.

I/O Ports

The SM5K6/5K7 have 24 ports, 4 input and 20 I/O ports. Some ports assume additional port functions.

- External interrupt input
- Standby release
- Count clock input
- Analog voltage input (A/D)
- SIO (serial interface)

Port P0

This is a 4-bit I/O port, all 4 bits can be set the same direction. When set as output, the port can accommodate up to 15 mA (TYP.) sink current. When used in conjunction with P1 port, the P0 delivers one half an 8-bit data.

Port P1

This is a 4-bit I/O port, all 4 bits can be set the same direction. When set at output, the port can accommodate up to 15 mA (TYP.) sink current. When used in conjunction with P0 port, the P1 delivers one half an 8-bit data.

Port P2

This is a 4-bit I/O port. Each bit can be independently set its direction. Each pin of the port can also assume the following function pin.

- $P2_0$ and $P2_1$ pins – external interrupt input, standby release.
- $P2_2$ – count clock input, standby release.
- $P2_3$ – buzzer output, standby release.

Port P3

This is a 4-bit input port. It can serve as A/D pin in addition to a general purpose input pin.

Port P4

This is a 4-bit I/O port. Direction of each bit can be independently set. Each pin of the port can also assume the following function pin.

- $P4_0$ – A/D pin, serial data input.
- $P4_1$ – A/D pin, serial data output.
- $P4_2$ – A/D pin, serial clock I/O
- $P4_3$ – A/D pin

Port P5

This is a 4-bit I/O port, all four pins can be set to the same direction.

$\overline{\text{RESET}}$ Pin

Input to this pin initializes the microcomputer (hardware reset). Normal configuration is to connect a capacitor across $\overline{\text{RESET}}$ and GND pins so that the hardware reset automatically starts upon power-up. Do not leave $\overline{\text{RESET}}$ pin open.

Placing a LOW level on the $\overline{\text{RESET}}$ pin starts hardware reset of the SM5K6/5K7. For further information, see ‘Hardware Reset’ in the Functional Description.

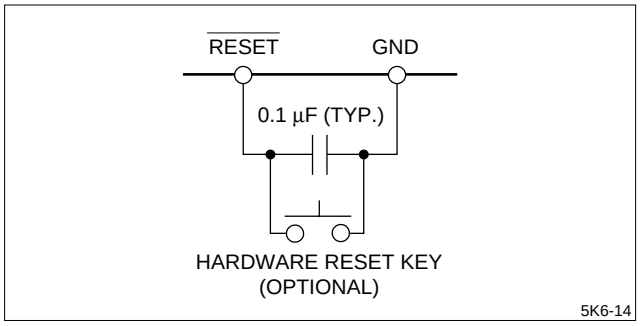


Figure 14. Power-on Reset Circuit

OSC_{IN}, OSC_{OUT} Pins

Connecting required external components (crystal, etc.) to these pins configures the main clock oscillator.

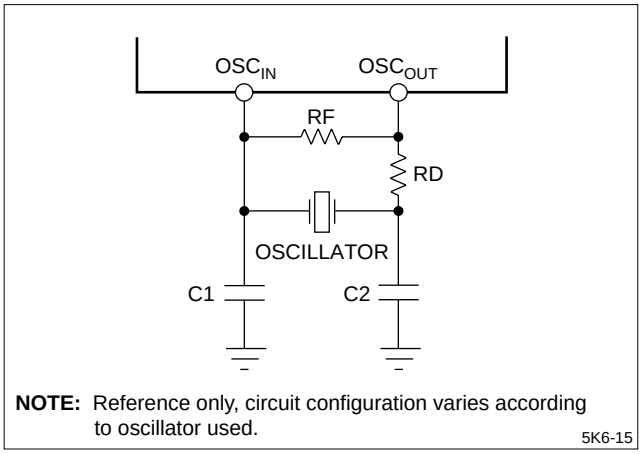


Figure 15. Main Clock Oscillator Circuit (Under Evaluation)

V_{DD}, GND, VR and AGND Pins

These pins supply power to the SM5K6/5K7. V_{DD} and GND supply the system power, VR and AGND supply the reference voltage to the internal A/D converter.

GND pin should be connected to AGND. Across V_{DD} and GND, connect an electro capacitor to absorb external noise. Although VR can be separately supplied (2.0 V to V_{DD}), it should be derived from V_{DD} for the best precise A/D conversion.

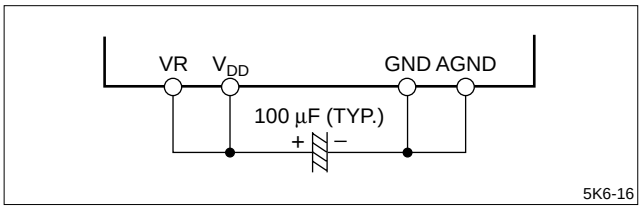


Figure 16. Recommended Power Supply Connection

Flags

The SM5K6/5K7 have six flags (C flag and interrupt demand flag of IFA, IFB, IFT1, IFT2, and IFS) which are used to setting condition and judgement.

System Clock Generators and Dividers

System Clock Generator

The system clock generating system is shown in Figure 17. The system clock f_{SYS} is the divided-by-4 main clock applied through OSC_{IN} and OSC_{OUT}. See Figure 18 for frequency relationship between these two clocks. To complete the main clock oscillator, external components must be connected between OSC_{IN} and OSC_{OUT} pins.

Execution time of one byte one cycle instruction is equal to one system clock period. The system clock (f_{SYS}) frequency is 1 MHz and the instruction execution time is 1 µs per cycle when the clock is derived from the 4 MHz ceramic.

The system clock frequency is 8,192 Hz and the instruction execution time is 122 µs per cycle when the clock is derived from the 32.768 kHz crystal. The system clock f_{SYS} is also used as the count pulse input to the timer.

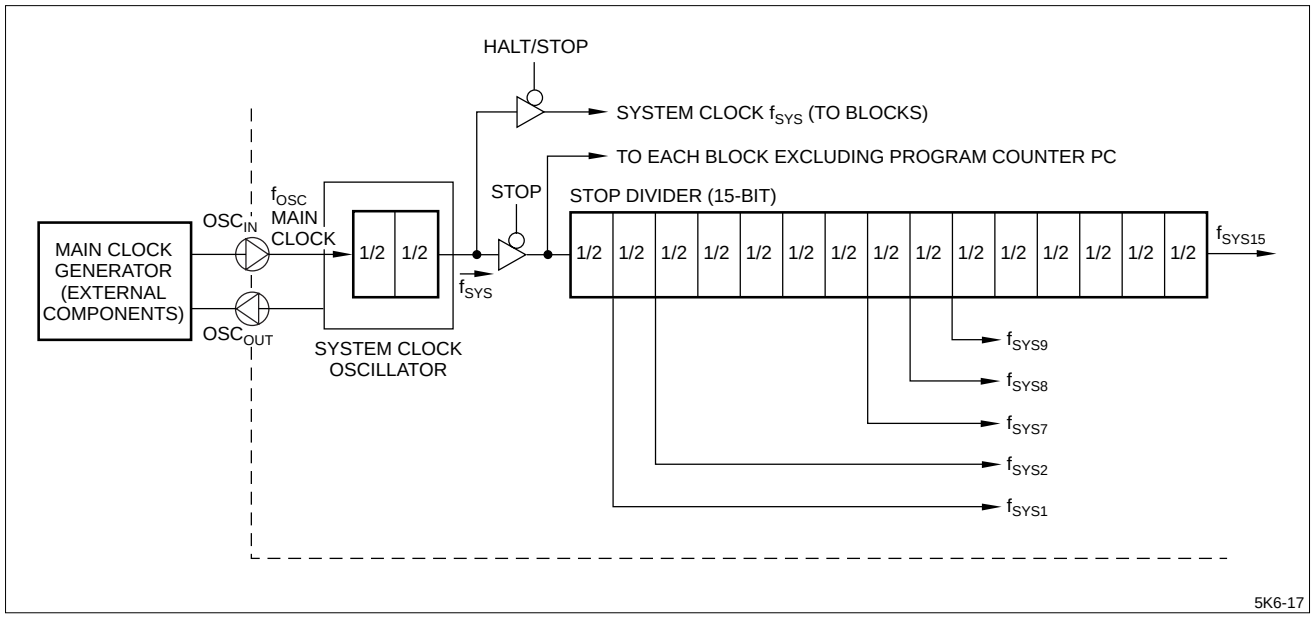


Figure 17. System Clock Generator and Divider

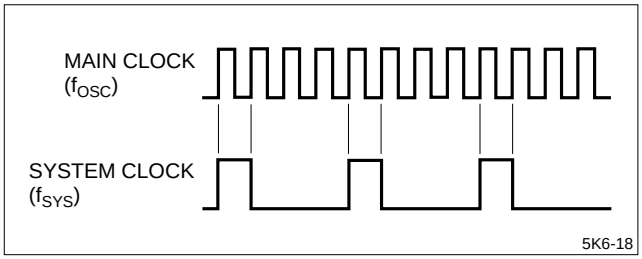


Figure 18. Main Clock and System Clock

Divider (DIV)

The divider consists of 15-step divider circuits and produces the following 6-clock from the system clock. These divided clocks are provided for timer/counters, serial interface and buzzer output. All steps of the divider can be cleared by DR instructions.

Resonator Mask Option

Selection of type of resonator, i.e. ceramic or crystal is made by masked option.

Table 2. Divider Output Clock Versus f_{SYS}

SYMBOL	CLOCK
f_{SYS}*	System clock
f_{SYS1}	Divided-by-2 system clock (output of 1st step)
f_{SYS2}	Divided-by-4 system clock (output of 2nd step)
f_{SYS7}	Divided-by-128 system clock (output of 7th step)
f_{SYS8}	Divided-by-256 system clock (output of 8th step)
f_{SYS9}	Divided-by-512 system clock (output of 9th step)
f_{SYS15}	Divided-by-32,768 system clock (output of 15th step

FUNCTION DESCRIPTION

Hardware Reset Function

The hardware reset initializes the SM5K6/5K7 system. The hardware reset (power-on reset) starts upon power up. When the timer 2 is used as a watch dog timer, it also starts the hardware reset circuit as it overflows.

Hardware Reset and System Status

The $\overline{\text{RESET}}$ pin is at HIGH level while the SM5K6/5K7 are operating normally. When the level is forced to LOW externally, the hardware reset sequence starts after two instruction cycles. When the level on the $\overline{\text{RESET}}$ pin returns to HIGH, the SM5K6/5K7 start counting the main clock which is oscillating between OSC_{IN} and OSC_{OUT}. As a count about 2^{14} is reached, the system exits hardware reset status and the program starts at address 0 in page 0.

Table 3. Status of the System Immediately After Hardware Reset

PARAMETER		VALUE OR STATUS
All I/O ports (input and I/O ports)		Input mode with pull-up resistor connected
All control registers (except for SIO register R18)		0 (write only bits are also 0 when read into A register)
SIO shift register R18		Undefined
Functions	AD converter Interrupt Standby Timer/counter Serial interface Buzzer out	All inactive or disabled
Flags	C flag	Undefined
	Interrupt master enable flag IME	0 (all interrupts disabled)
	Interrupt request flag (IFA, IFB, IFT1, IFT2, IFS)	0
Others	A and X registers	Undefined
	Program counter PC (P_U, P_L)	0000_H
	B register (B_U*, B_M, B_L)	Undefined
	SB register (B_U*, B_M, B_L)	Undefined
	Stack register SR	Undefined
	Level of stack register SR	Level 1
	Contents of RAM	Undefined

NOTE: *SM5K7 only.

Standby Feature

Standby feature saves power by stopping the program whenever it is not necessary to run. The mode in which the microcomputer is executing the program is called run mode and the mode in which it stops the program is called standby mode.

Standby mode is further divided into two modes; stop mode and halt mode, one of which is selected by halt instruction or stop instruction. Upon removal of standby condition, the SM5K6/SM5K7 return from the standby mode to the normal run mode.

To enter the standby mode, select either stop mode or halt mode whichever is appropriate.

SYSTEM OPERATION AND STATUS DURING STANDBY MODE

Operations in Halt Mode

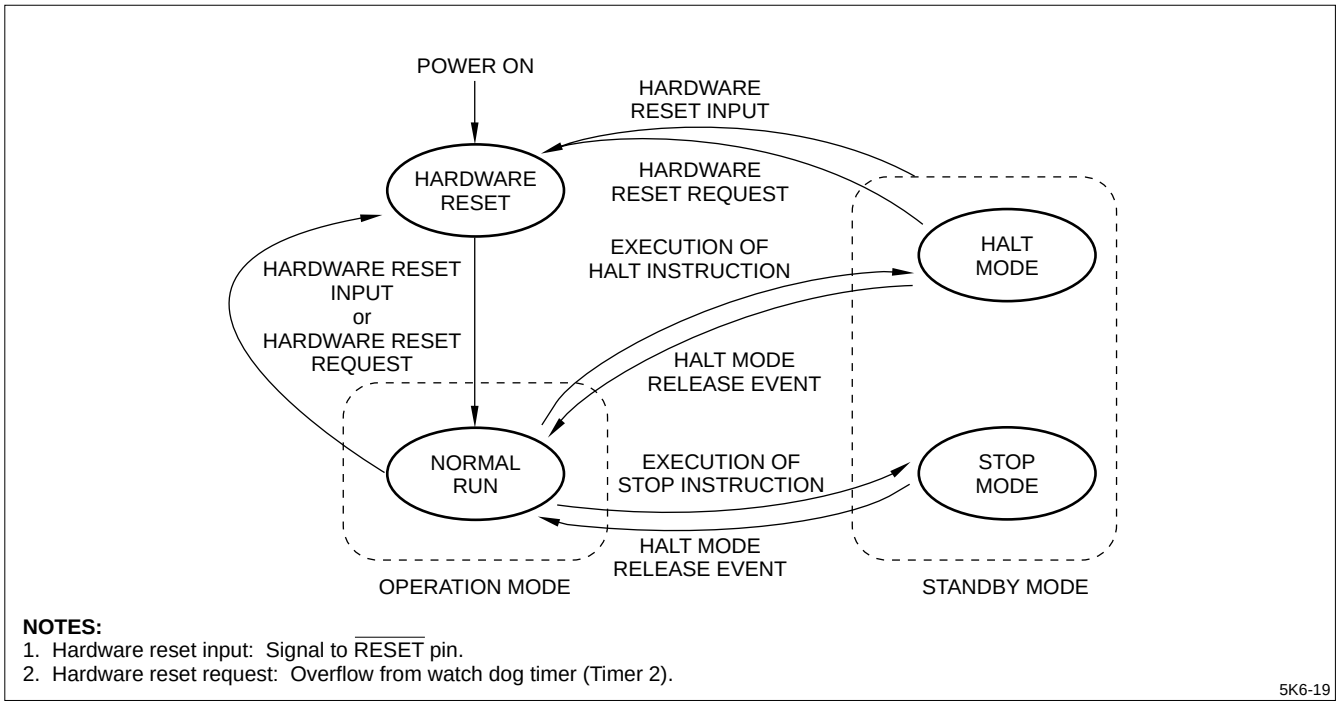
In the halt mode, the program counter PC stops to pause the program. The system clock f_{SYS} is still supplied to other functional blocks keeping the clocks driven by the clocks from the divider and external clock activated.

Operations in Stop Mode

In the stop mode, the main clock is stopped. This means that most of functional blocks are stopped. Exceptions; P2 port can recognize external input, and the serial interface can work if operated by external clock.

Table 4. Operation/Status in Halt/Stop Mode

FUNCTIONAL BLOCK	OPERATION/STATUS	
	HALT MODE	STOP MODE
Hardware reset	Recognized	Recognized
Timer 1	O	X
Timer 2	O	X
A/D converter	X	X
Serial interface	O	Operates only on external clock
Buzzer out	Same as before entering halt mode	Stop (level unconditional)
I/O port	Same as before entering half mode	Same as before entering stop mode



NOTES:
1. Hardware reset input: Signal to $\overline{\text{RESET}}$ pin.
2. Hardware reset request: Overflow from watch dog timer (Timer 2).

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Figure 19. Operation of Program

USE OF HALT MODE AND STOP MODE

The operation immediately returns from the halt mode to the normal mode as a halt mode release event occurs. Generally, the halt mode is used when the system repeatedly moves between the standby mode and run mode.

The stop mode saves more power than the halt mode but has some detrimental effects. Time required for the system to return to the normal run mode is longer (approximately 450 instruction cycles) than that of halt mode. Stop mode can be cancelled only by applying LOW level on P2 port, SIO operating on an external clock or hardware reset. The stop mode is best suitable when the system stays for a longer period in the standby mode and does not require fast returning to the normal run mode. The standby mode retains I/O port settings and levels on the output ports as they are. Program should be prepared so that currents flowing to/from pins are reduced before the SM5K6/5K7 are put into the standby mode.

SETTING AND OPERATION OF STANDBY

Table 5. Standby Release Events (8-Type)

RELEASING EVENT	MASKABLE	PRIORITY LEVEL	FLAG	APPLICABLE IN STOP MODE
Hardware reset input	No	—	—	Yes
LOW level on $P2_0$	Yes	1	IFA	Yes
LOW level on $P2_1$	Yes	3	IFB	Yes
LOW level on $P2_2$	Yes	—	—	Yes
LOW level $P2_3$	Yes	—	—	Yes
End of SIO transfer	Yes	3	IFS	No
Interrupt request flag IFT1 is 1 (timer 1 overflow)	Yes	2	IFT1	No
Interrupt request flag IFT2 is 1 (timer 2 overflow)	Yes	4	IFT2	No

Interrupt Feature

The interrupt block consists of interrupt enable flags (bits of control register RE and interrupt master enable flag IME), interrupt request flags (IFA, IFB, IFT1, IFT2 and IFS) and interrupt handing circuit.

Interrupts Used with SM5K6/SM6K7

Although the SM5K6/5K7 are provided with five interrupts, four interrupts are set at the same time because $P2_1$ selectively uses one of two. When an interrupt occurs the corresponding interrupt request flag (IFA, IFB, IFT1, IFT2, IFS) is set '1' level.

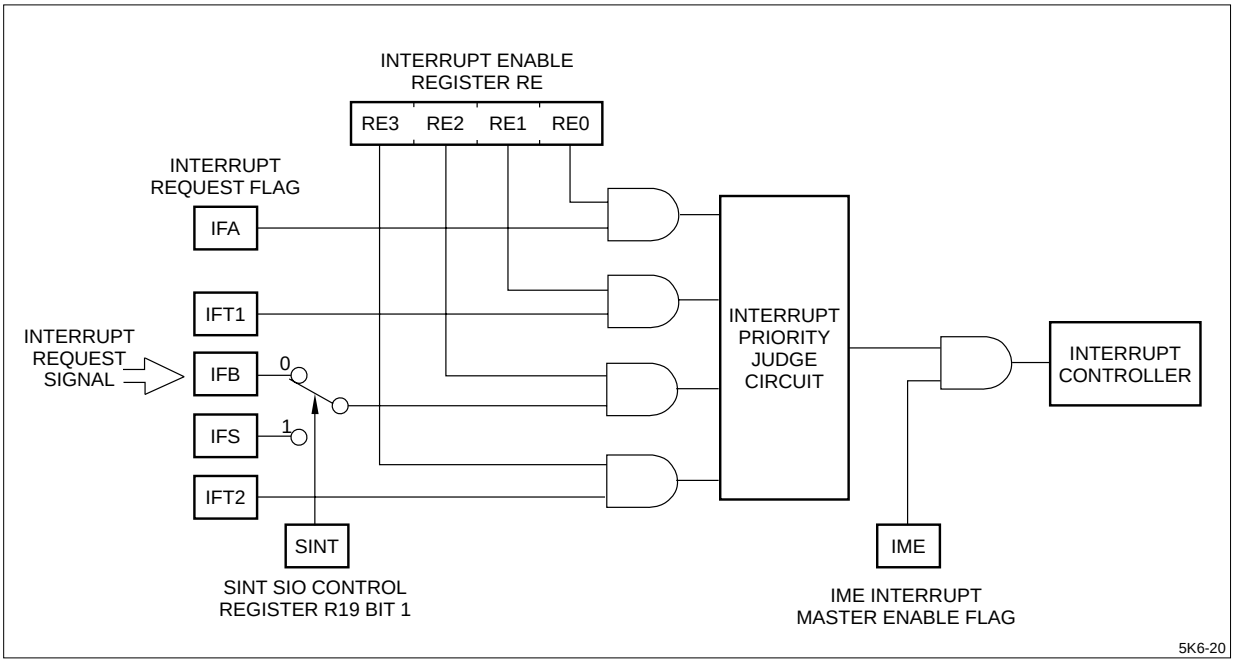

Figure 20. Interrupt Block Diagram

Disabling All Interrupt Requests (IME Flag)

The interrupt master enable IME is the flag which inhibits all interrupt. The execution of IE instruction sets the IME flag to '1', enabling the interrupt set by the interrupt enable register RE. In contrast, the ID instruction sets the IME flag to '0' and disables all interrupt requests.

Enabling and Disabling Individual Interrupt Requests (Interrupt Enable Register RE)

The interrupt enable register RE (RE0, RE1, RE2, RE3, interrupt mask flag) enable and disables each of five interrupts. Each bit of RE is called mask flag.

Timer/Counter

The SM5K6/5K7 have two paris of built-in timer/counters. These counters are used to handle periodic interrupts and to count external events. The overflowing timer can be used to disable the halt mode. The timer/counters serve as interval counter. In addition, the timer 2 can be used as watch dog timer (overrun detect timer). Each timer/counter consists of an 8-bit count register, modulo register and 4-bit timer control register.

Table 6. Interrupt Event Summary

INTERRUPT EVENT	FLAG	CORRESPONDING BIT OF RE	JUMP ADDRESS		PRIORITY LEVEL
			PAGE	STEP	
$P2_0$ interrupt (falling edge on $P2_0$)	IFA	RE0	02_H	00_H	1
Timer 1 interrupt (timer 1 overflow)	IFT1	RE1	02_H	02_H	2
$P2_1$ interrupt (falling edge on $P2_1$)	IFB	RE2*	02_H	04_H	3
SIO interrupt (end of serial interface operation)	IFS	RE2*	02_H	04_H	3
Timer 2 interrupt (timer 2 overflow)	IFT2	RE3	02_H	06_H	4

NOTE: *One of $P2_1$ or SIO interrupts is selected by bit 1 of SIO control register R19. $P2_1$ interrupt – R19 bit 1 = 0, SIO interrupt – R19 bit 1 = 1.

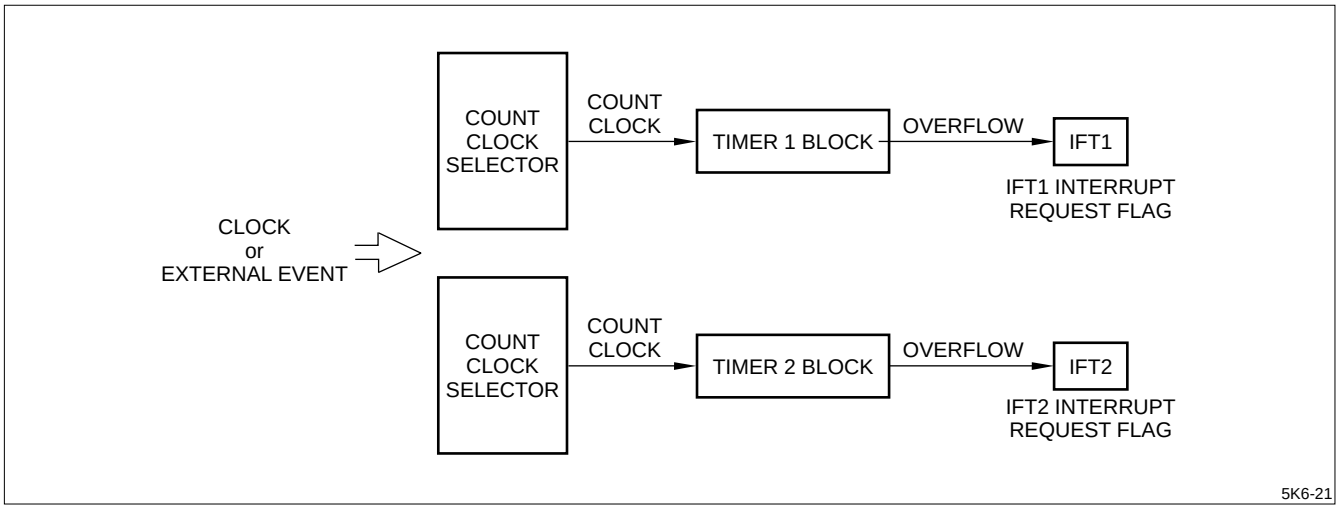

Figure 21. Configuration of Timer/Counter

TIMER 1

The Timer 1 is an 8-bit timer/counter. It counts a divided-by-n system clocks and external events. Figure 22 shows a block diagram of the Timer 1. Timer 1 has no watch dog timer capability which timer Timer 2 has, although both timers have the same configuration. Selectable clocks are also different between both timers.

Selecting Count Clock

Selects the count clock by setting bits of the control register R0C.

Table 7. Selection of Count Clock

REGISTER R0C BITS		SELECTED COUNT CLOCK
$R0C_1$	$R0C_0$	
0	0	f_{SYS} (system clock)
0	1	f_{SYS7} (divided-by-7 system clock)
1	0	f_{SYS15} (divided-by-15 system clock)
1	1	External clock (falling edge on $P2_2$). When set external clock pin, $P2_2$ does not act as the standby release pin. This means that SM5K6/5K7 can count the external clock while in the halt mode. For further information, refer to 'Standby Feature'.

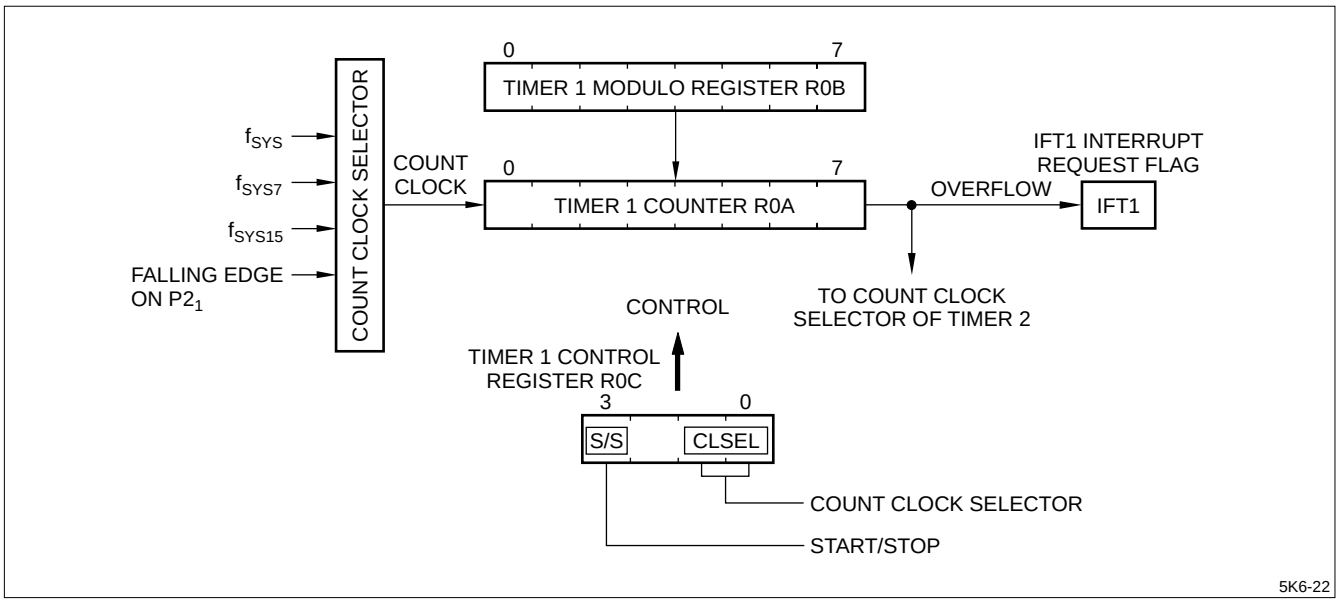

Figure 22. Timer 1 Block

TIMER 2

The Timer 2 is an 8-bit timer/counter. It counts a divided-by-n system clocks. Figure 23 shows a block diagram of the Timer 2. Timer 2 has watchdog timer capability which the timer 1 does not, although both timers have the same configuration. Selectable clocks are also different between both timers.

Selecting Count Clock

Selects the count clock by bit setting of the control register R1C. Selecting the overflow from the Timer 1 as the count clock source connects the Timer 2 to Timer 1 in the cascade fashion, a single 16-bit timer.

Selecting Operation Mode

The Timer 2 can be used as a watchdog timer by the following mode setting.

- Use as a normal timer, control register R1C, bit 2 ← store '0'.
- Use as a watchdog timer, control register R1C, bit 2 ← store '1'.

This setting is made valid when done at the beginning of timer start.

To Use the Timer 2 as the Watchdog Timer

Watchdog timer is also called overrun detect timer because it informs the CPU that the CPU is in a closed loop and overrunning due to some trouble, for example, program error. The overflowing watchdog timer starts the hardware reset sequence.

The program must write the initial value to the watchdog timer at an interval before the watchdog overflows. Therefore, an overflow from the watchdog timer means that the program is not running normal, for example, it is in an endless loop.

Table 8. Selection of Count Clock

REGISTER R1C BITS		SELECTED COUNT CLOCK
$R1C_1$	$R1C_0$	
0	0	f_{SYS} (system clock)
0	1	f_{SYS7} (divided-by-7 system clock)
1	0	f_{SYS15} (divided-by-15 system clock)
1	1	Timer 1 overflow

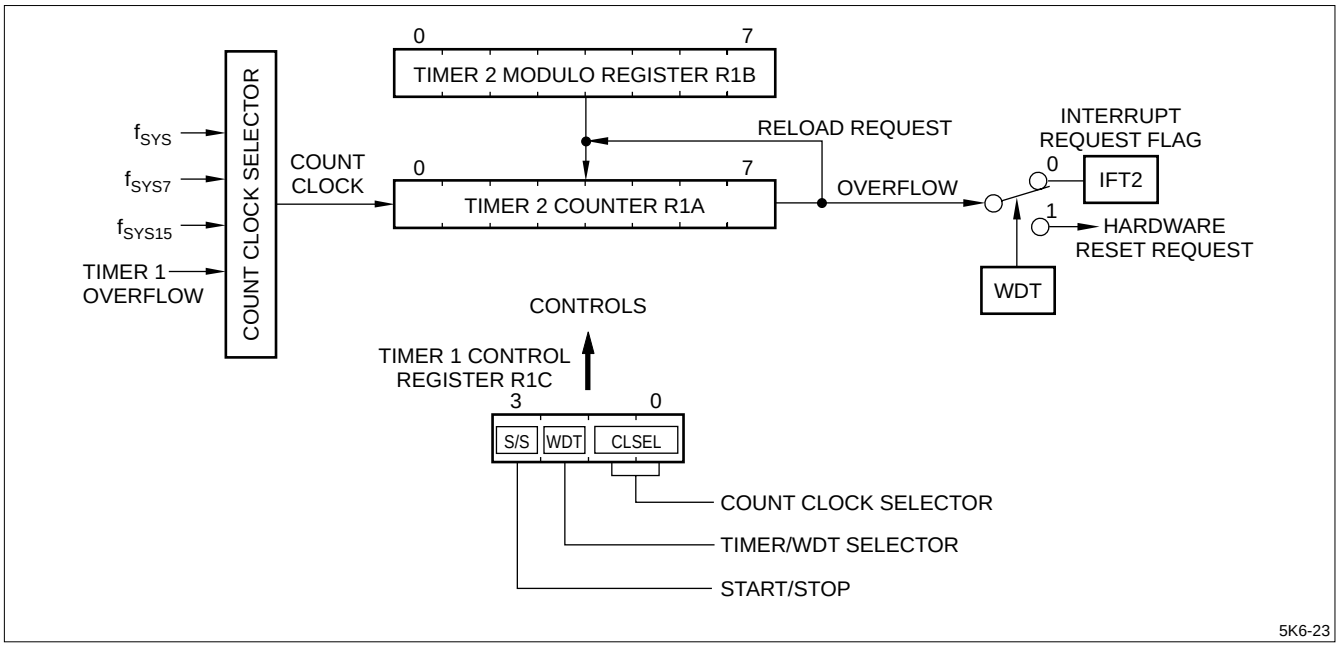

Figure 23. Timer 2 Block

A/D Converter

The SM5K6/5K7 internal 10-bit A/D converter is provided with eight input channels and operates either in the A/D conversion mode or comparison mode. The A/D converter mode converter mode converts the analog voltage coming through P3 and P4 ports to the equivalent digital value. The comparison mode compares the level of the input analog voltage with the voltage level set within the SM5K6/5K7 and stores the result in the microcomputer.

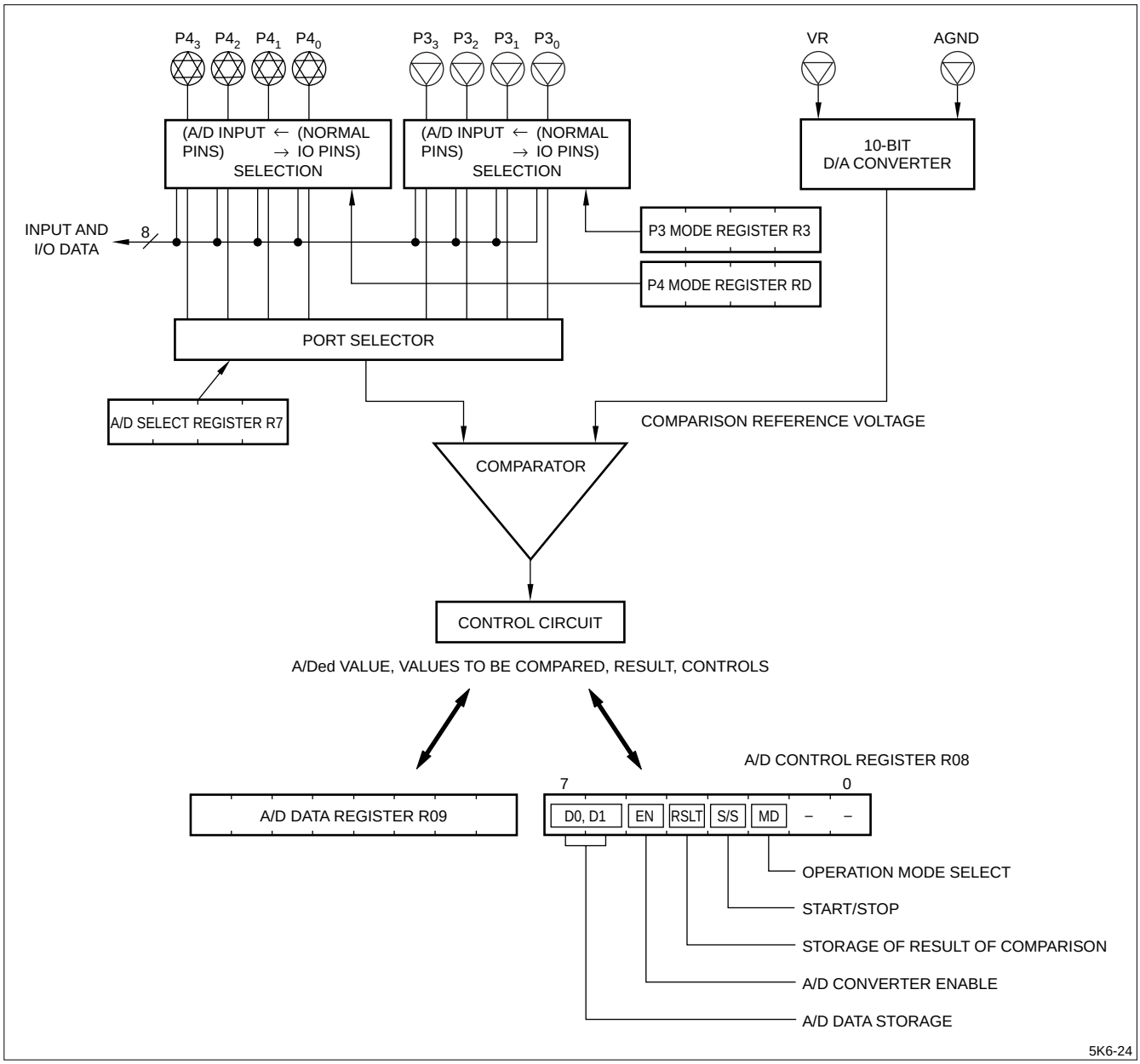

Figure 24. Block of A/D Converter

A/D CONVERSION MODE

The A/D conversion mode converts the analog voltage on A/D pin into the digital value. The input analog voltage is successively compared with weighted voltages from the capacitor array. Digitized conversion data (10-bit) are stored into upper two bits places of the control register R08 and the remaining bits into the data register R09.

The time required for the converter to complete conversion is as follows:

- Conversion duration = system clock period × 30.5
  - 30.5 µs (main clock at 4 MHz/1 µs system clock)
  - 305 µs (main clock at 400 kHz/10 µs system clock).

CAUTION

While in the A/D conversion mode, do not use registers (upper 2 bits of R08 register and the R09 register) reserved for storage of A/D data to store other data.

NOTES:

1. Apply voltage within the range between 2.0 V and V_{DD} level to the VR pin; the A/D converter reference voltage pin. Do not apply a voltage outside this range.
2. Don't apply the voltage VR pin before feeding V_{DD} pin.
3. AGND pin must be connected to GND pin.

Serial Interface

The SM5K6/5K7 have an 8-bit synchronous serial interface which transfers 8-bit data stream synchronously with the external and internal clock.

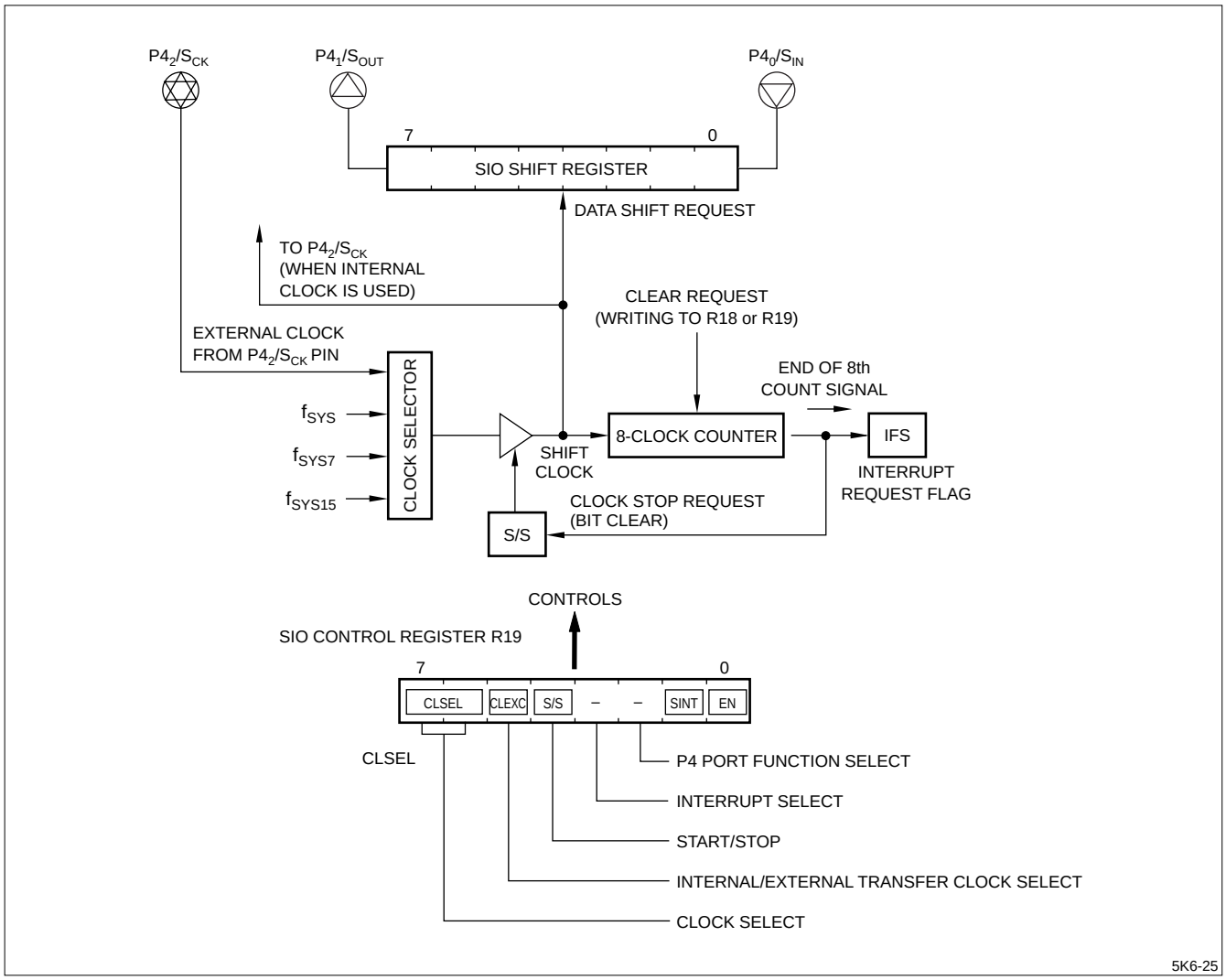

Figure 25. Serial Interface Block

OPERATION AND CONTROL SIO

Transfer Timing

Transfers the contents of the shift register R18 to S_{OUT} pin on the falling edge of the transfer clock and then transfers the level on S_{IN} pin to the shift register R18 on the rising edge of the next transfer clock. Transmitted data is output MSB first and received data is input LSB first.

At the end of transfer, the oldest bit data is shifted to the MSB position of the shift register R18 and the latest data in the LSB position.

Transfer Start Timing

The SM5K6/5K7 starts transfer on the first rising edge of the transfer clock after S/S is set.

Range of Time Delay from the Start of the Transfer to the Rising Edge of the Next Transfer Clock

When the internal clock is selected as the transfer clock, the time from the falling edge of the transfer clock immediately after the start of the transfer to the rising of the next transfer clock depends on the start timing of the transfer. The minimum delay is equivalent to 1/4 f_{SYS} cycle (3/4 f_{SYS} cycle if f_{SYS} is used as the transfer clock) and maximum is approximately 1/2 clock cycle. These delay variations should be taken into consideration in applying SIO data to S_{IN} pin. To minimize delay variations, clear the divider immediately before the start of SIO.

Data Output Timing

The data output timing refers to the moment at which bits of the shift register are clocked out on S_{OUT} pin. Upwarding arrows in the diagram show output data shifting timing. Waveform numbers (1 to 8) in Figure 26 indicate data output order (shift register bit 7 first, 0 last). The timing of latching the level on S_{OUT} pin to the external circuit should be determined by the external system connected to the SM5K6/5K7 based on the clock of S_{CK} pin.

Input Data Latch Timing

This is the duration in which SM5K6/5K7 latch S_{IN} level to store the data into the shift register. This timing should also be determined by the external transferring device, based on the transfer clock.

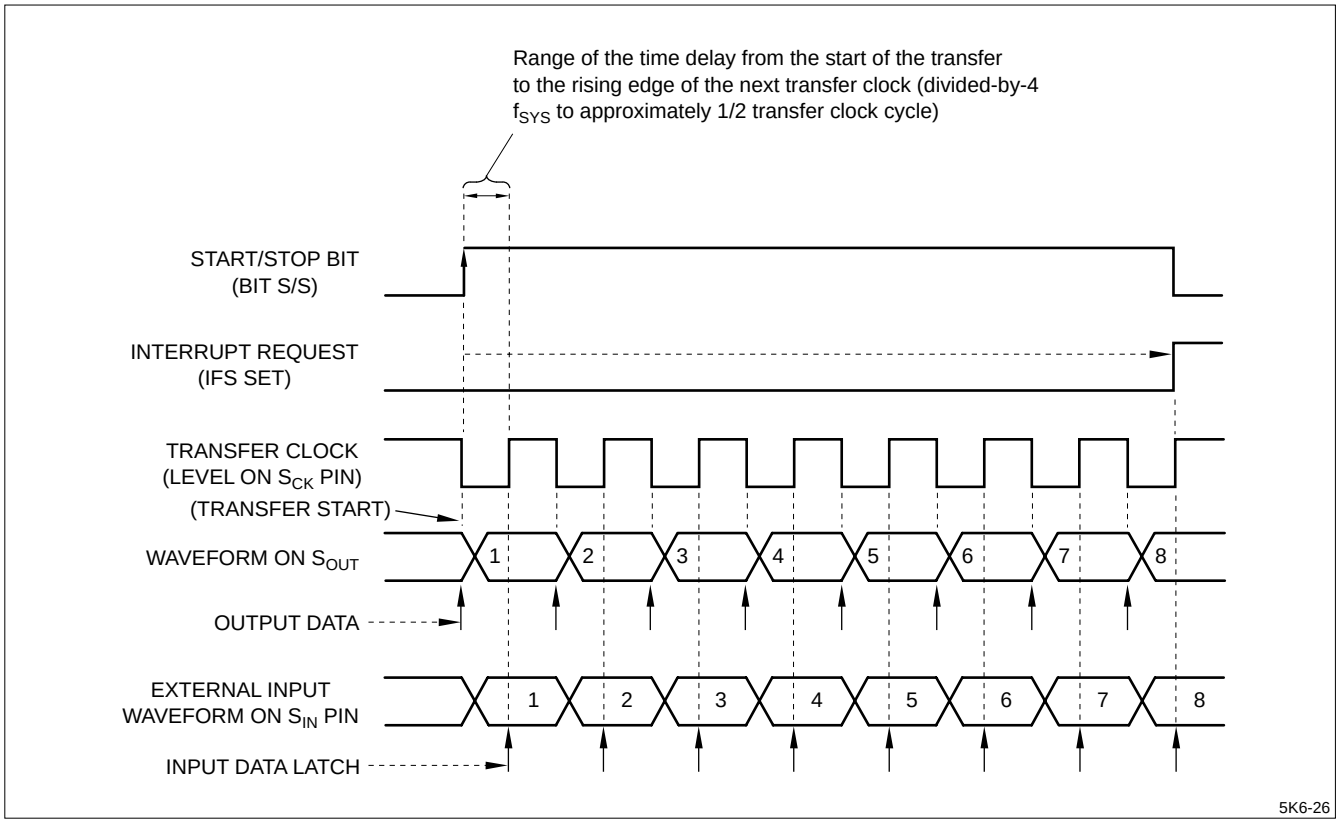

Figure 26. SIO Transfer Timing Chart

Buzzer Output

The SM5K6/5K7 generate four buzzer drive clocks, one of which is selected and placed on $P2_3$ pin.

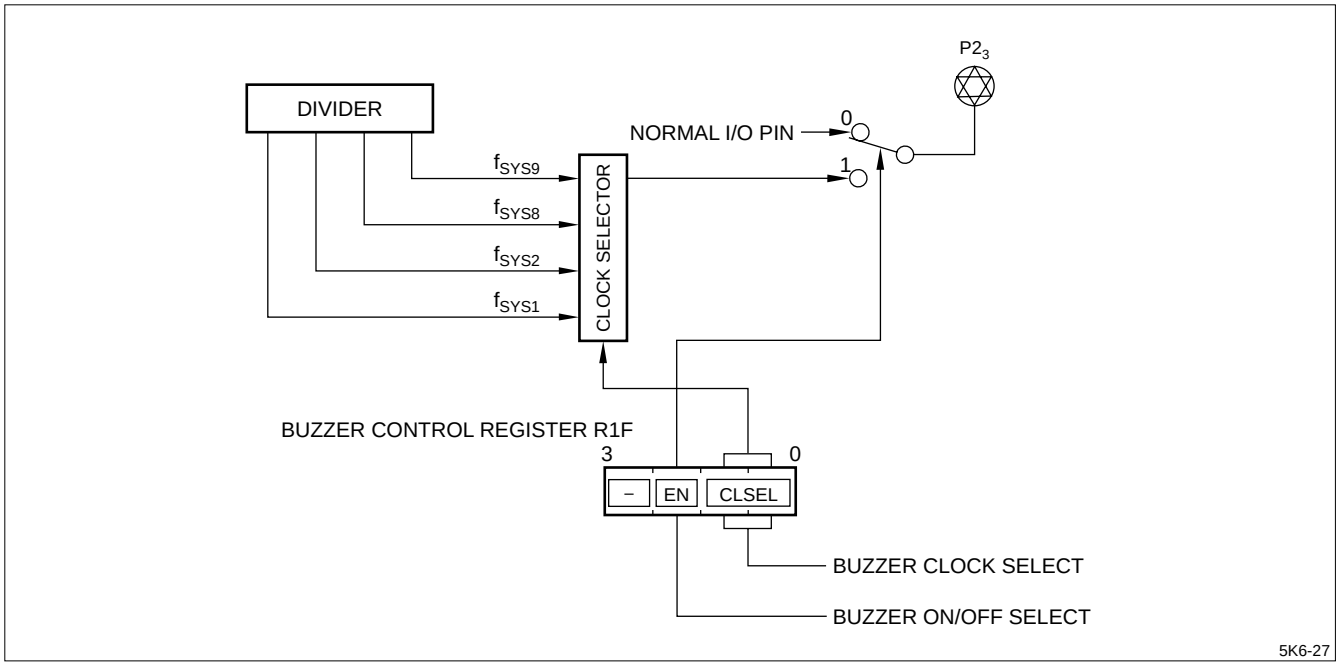

Figure 27. Buzzer Output Block

CONTROL REGISTER SET

Control Register Summary

Table 9 shows the configuration of control registers and settings of the B register which allows access to control register.

Table 9. Control Registers

B REGISTER SETTING		CONTROL REGISTER NUMBER	NAME	CONFIGURATION
BM	BL			
*	0	P0	P0 port	———
			P0 register	P03 P02 P01 P00
*	1	P1	P1 port	———
			P1 register	P13 P12 P11 P10
*	2	P2	P2 port	———
			P2 register	P23 P22 P21 P20
*	3	P3	P3 port	———
		R3	P3 mode register	MD33 MD32 MD31 MD30
*	4	P4	P4 port	———
			P4 register	P43 P42 P41 P40
*	5	P5	P5 port	———
			P5 register	P53 P52 P51 P50
*	6	R6	P4 direction register	DR43 DR42 DR41 DR40
*	7	R7	A/D select register	– ADSEL
0	8	R08	A/D control register	D1. D0 EN RSLT S/S MD –
0	9	P09	A/D data register	D9 D8 D7 D6 D5 D4 D3 D2
0	A	R0A	Timer 1 counter	D7 D6 D5 D4 D3 D2 D1 D0
0	B	R0B	Timer 1 modulo register	D7 D6 D5 D4 D3 D2 D1 D0
0	C	R0C	Timer 1 control register	S/S – CLSEL
*	D	RD	P4 mode register	MD43 MD42 MD41 MD40
*	E	RE	Interrupt enable register	IE3 IE2 IE1 IE0
0	F	R0F	P2 direction register	DR23 DR22 DR21 DR20
1	8	R18	SIO shift register	D7 D6 D5 D4 D3 D2 D1 D0
1	9	R19	SIO control register	CLSEL CLEXC S/S – SINT EN
1	A	R1A	Timer 2 counter	D7 D6 D5 D4 D3 D2 D1 D0
1	B	R1B	Timer 2 modulo register	D7 D6 D5 D4 D3 D2 D1 D0
1	C	R1C	Timer 2 control register	S/S WDT CLSEL
1	F	R1F	Buzzer control register	– EN CLSEL

NOTE: * Don't Care

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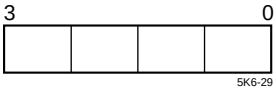
R3 (P3 Mode Register)

P3 mode register R3 sets the operation mode of P3 port (general purpose input or A/D port). The pull-up resistor is disconnected from the A/D pin which then cannot be used as a general purpose input pin. When connecting A/D pins to the A/D converter, one of the A/D pins must be set (by the corresponding bit of the A/D select register R7) to the analog voltage input pin.



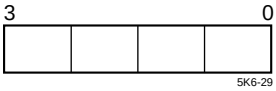
Bit i (i = 3 to 0): Mode Select Bits

These bits set P3i pin to either general purpose input or A/D pin.

BIT	CONTENT
0	(General purpose) input
1	A/D input

R6 (P4 Direction Register)

P4 direction register R6 sets P4 port to input or output. P4 port also assumes A/D port and SIO I/O port. While P4 port is used as A/D or SIO port, it cannot be changed to input or output port even though direction of P4 is set by setting R6 (setting is established but ignored).



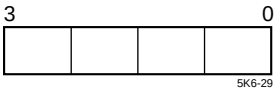
Bits i (i = 3 to 0): Direction Switch Bit

These bits switch the direction of P4i.

BIT	CONTENT
0	Input
1	Output

R7 (A/D Select Register)

The A/D select register R7 selects the A/D converter input pin among the A/D pins. Eight pins among P3 and P4 port should be set as A/D pins before setting R7. A pin other than A/D pins should not be selected as A/D converter input pin. To select A/D pins, use the P3 mode register R3 and P4 mode register RD.



Bit 3: Unused

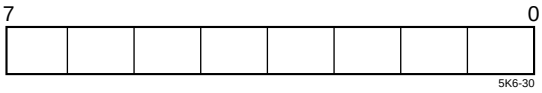
Bits 2: to 0 A/D Pin Select Bits

These bits select one of eight pins.

BIT	CONTENT	BIT	CONTENT
000	$P3_0$	100	$P4_0$
001	$P3_1$	101	$P4_1$
010	$P3_2$	110	$P4_2$
011	$P3_3$	111	$P4_3$

R08 (A/D Control Register)

The A/D control register R08 stores controls of A/D converter and part of A/D data.



Bits 7 to 6: A/D Data Storage Bits

These bits store the A/D data (two low bits out of ten bits) after conversion while in the A/D conversion mode or the internal voltage set value with in the comparison mode.

Bit 5: A/D Converter Enable Bit

To enable A/D converter set this bit to ‘1’ level upon power-up. The bit is automatically cleared to ‘0’ at the end of conversion.

BIT	CONTENT
0	Disable
1	Enable

Bit 4: Comparison Result Storage Bit

This bit stores the result of comparison when the A/D converter is operating in the comparison mode. When the pin voltage becomes equal to the internal set voltage, level of this bit is unconditional.

BIT	CONTENT
0	Pin voltage < internal set voltage
1	Pin voltage > internal set voltage

Bit 3: Start/Stop Bit

When at ‘1’ level, the bit starts A/D converter and remains ‘1’ level and becomes ‘0’ at the end of conversion and remains ‘0’ until next conversion starts. Monitoring this bit status is to monitor A/D operation.

BIT	CONTENT
0	Not in operation
1	In operation

Bit 2: Operation Mode Select Bit

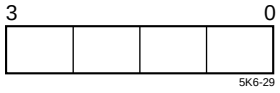
Changes the operation mode of A/D converter.

BIT	CONTENT
0	A/D conversion
1	Comparison

Bits 1 to 0: Unused

R0C (Timer 1 Control Register)

Timer 1 control register selects the count clock for the Timer 1 and starts and stops the timer. Difference between Timer 1 and Timer 2: types of count clocks selectable. Timer 2 has watchdog timer capability.



Bit 3: Timer 1 Start/Stop Bit

Starts and stops the Timer 1 up count.

BIT	CONTENT
0	Stops, in stop
1	Count starts, in operation

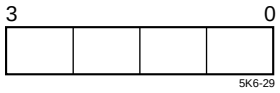
Bit 2: Unused

Bits 1 to 0: Timer 1 Count Clock Select Bits

BIT	CONTENT
00	f_{SYS} (system clock)
01	f_{SYS7} (divided-by-7 system clock)
10	f_{SYS15} (divided-by-15 system clock)
11	$P2_2$ falling edge

RD (P4 Mode Register)

P4 mode register RD sets P4 mode to either general purpose I/O pin or A/D pin. The pin set A/D is disconnected from the pull-up resistor. Once set A/D port by RD, P4 cannot act as general purpose I/O or SIO port. To use P4 as I/O or SIO port, set again the mode register RD for desired P4 mode. To use A/D pins for A/D converter, set one of A/D pins to the analog voltage input pin by setting the bit of the A/D select register R7.



Bit i (i = 3 to 0): Mode Select Bit

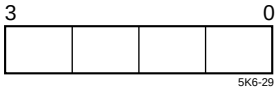
These bits set P4i pin to general purpose I/O pin or A/D pin.

BIT	CONTENT
0	General purpose I/O pin
1	A/D input

RE (Interrupt Enable Register)

Interrupt enable register RE enables/disables individual interrupts. This register should be set in conjunction with the interrupt master enable flag IME (ID/IE instruction). When an interrupt is initiated, the corresponding interrupt request flag is set '1'. This and other interrupt request flags are not assigned to any control registers but separately provided. The status of each interrupt request flag can be identified by executing a specific instruction.

INTERRUPT	FLAG SYMBOL	INSTRUCTION	INTERRUPT ENABLE REGISTER BIT
$P2_0$ interrupt	IFA	TA	IE0
$P2_1$ interrupt	IFB	TB	IE2
Timer 1 interrupt	IFT1	TT1	IE1
Timer 2 interrupt	IFT2	TT2	IE3
SIO interrupt	IFS	TSF	IE2



Bit 3: Timer 2 Interrupt Enable Bit

Enables the interrupt initiated by Timer 2 overflow.

BIT	CONTENT
0	Disable
1	Enable

Bit 2: $P2_1$/SIO Interrupt Enable Bit

Enables the interrupt initiated by the falling edge input on $P2_1$ or the interrupt initiated at the end of SIO (serial interface). One of these interrupt events must be selected by the setting of SIO control register R19 because only one of the events is used at a time.

BIT	CONTENT
0	Disable
1	Enable

Bit 1: Timer 1 Interrupt Enable Bit

This bit enables initiated upon Timer 1 overflow.

BIT	CONTENT
0	Disable
1	Enable

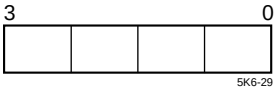
Bit 0: $P2_0$ Interrupt Enable Bit

Enables interrupt from $P2_0$ initiated on falling edge on this pin.

BIT	CONTENT
0	Disable
1	Enable

R0F (P2 Direction Register)

P2 direction register R0F sets the direction of P2 port. P2 port can also assume input or output as set even if it is set as a functional port. For example, the level on this port can be read by using an input instruction, while it is set as count clock input. When $P2_3$ is set the buzzer out, it outputs the buzzer clock as instructed to do so by the buzzer control register R1F.



Bit 3: $P2_3$ Direction Switch Bit

This bit switches the direction of $P2_3$.

BIT	CONTENT
0	Input (standby release)
1	Output (buzzer out)

Bit 2: $P2_2$ Direction Switch Bit

This bit switches the direction of $P2_2$.

BIT	CONTENT
0	Input (standby release, count clock input)
1	Output

Bit 1: $P2_1$ Direction Switch Bit

This bit switches the direction of $P2_1$.

BIT	CONTENT
0	Input (standby release, external interrupt)
1	Output

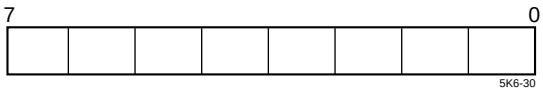
Bit 0: $P2_0$ Direction Switch Bit

This bit switches the direction of $P2_0$.

BIT	CONTENT
0	Input (standby disable, external interrupt)
1	Output

R19 (SIO Control Register)

Executing OUT instruction on SIO control register clears eight clock counters (reading serial clock eight times). The same operation occurs if the OUT instruction is given to SIO shift register. These operations assure 8-bit data transfer upon continuing of SIO after interruption of SIO. $P2_1$ interrupt and SIO interrupt cannot be enabled at a time. End of SIO operation can be verified by '1' IFS flag through TSF instruction, if SIO interrupt cannot be used.



Bits 7 to 6: SIO Transfer Clock Select Bit

BIT	CONTENT
00	f_{SYS} (system clock)
01	f_{SYS7} (divided-by-7 system clock)
10	f_{SYS15} (divided-by-15 system clock)
11	Timer 1 overflow

Bit 5: SIO Transfer Clock External/Internal Select Bit

Selects external source or internal source for transfer clock. Selection of external clock source disables setting of bits 7, 6 (SIO transfer clock select). Selection of the internal clock enables transfer of the internal clock to $P4_2/S_{CK}$ pin while SIO is running.

BIT	CONTENT
0	External clock
1	Internal clock

Bit 4: SIO Start/Stop Bit

When the internal transfer clock is selected, SIO starts upon setting of this bit to '1'. When the external transfer clock, the first external clock after setting this bit to '1' starts the SIO. Upon counting eight serial clocks, SIO stops and the external transfer clock is no longer catered for.

BIT	CONTENT
0	Stop (no transfer clock catered for)
1	Start (operation)

Bit 3 to 2: Unused

Bit 1: SIO Interrupt Select Bit

Either $P2_1$ interrupt (falling edge) or SIO interrupt is used at a time. This bit selects either interrupt.

BIT	CONTENT
0	$P2_1$
1	SIO

Bit 0: P4 Port Function Select Bit

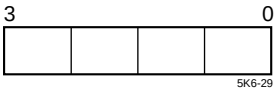
This bit sets $P4_0$, $P4_1$ and $P4_2$ to general purpose I/O pin or SIO pin.

BIT	CONTENT
0	$P4_0$, $P4_1$, $P4_2$ general purpose I/O
1	$P4_0$, $P4_1$, $P4_2$ S_{IN}, S_{OUT}, S_{CK}

R1C (Timer 2 Control Register)

Timer 2 control register selects the count clock for the Timer 2 and starts and stops the timer.

The difference between Timer 1 and Timer 2 are the types of count clocks selectable. Timer 1 lacks watchdog timer capability.



Bit 3: Timer Start/Stop Bit

Starts and stops the Timer 2 up count.

BIT	CONTENT
0	Stops, in stop
1	Count starts in operation

Bit 2: Timer Function Change Bit

Selects the application of Timer 2, timer or watchdog timer (WDT, overrun detect timer).

BIT	CONTENT
0	Standard timer
1	WDT (starts hardware reset sequence upon counter overflow)

Bits 1 to 0: Timer 2 Count Clock Select Bits

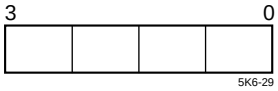
BIT	CONTENT
00	f_{SYS} (system clock)
01	f_{SYS7} (divided-by-7 system clock)
10	f_{SYS15} (divided-by-15 system clock)
11	Timer 1 overflow

R1F (Buzzer Control Register)

The buzzer control register R1F controls the clock placed on $P2_3$. This clock may also be used as an audio alarm. To use $P2_3$ as the buzzer output pin, set P2 direction register R0F for setting $P2_3$ as output pin. Once set buzzer, $P2_3$ output must be turned off and on by the bit 2 of the buzzer control register. Once the buzzer stops, P2 output latch register is output to $P2_3$ whose level should be adjusted.

Summary of Procedure

- Sets bit 3 of output latch register P2 to the desired level (determines the $P2_3$ output level during buzzer stop).
- Sets $P2_3$ to output pin by setting P2 direction register R0F.
- Sets bit of the buzzer control register to select the output clock.
- Turns on and off the buzzer output by the bit 2 setting of buzzer control register.



Bit 3: Unused

Bit 2: General Purpose Output/Buzzer Output Select Bit

Selects the function of $P2_3$.

BIT	CONTENT
0	Standard output (buzzer output stop)
1	Buzzer output

Bits 1 to 0: Output Clock Select Bits

Select clock to be output to $P2_3$.

BIT	CONTENT
00	f_{SYS9} (divided-by-9 system clock)
01	f_{SYS8} (divided-by-8 system clock)
10	f_{SYS15} (divided-by-15 system clock)
11	f_{SYS1} (divided-by-1 system clock)

Table 10. P4 Configuration

PIN	P4 DIRECTION SETTING BY REGISTER R6	SIO PIN CIRCUIT CONFIGURATION FOR SIO PIN (SIO STOP STATUS)
$P4_0/S_{IN}$	In (bit R60 ← 0)	Input with pull-up resistor
$P4_1/S_{OUT}$	Out (bit R61 ← 1)	CMOS output pin. Previous bit is output. Data unconditional after hardware reset.
$P4_2/S_{CK}$	Internal clock selected, out (bit $R6_2$ ← 1)	CMOS output pin (HIGH level)
	External clock selected, input (bit $R6_2$ ← 0)	Input pin with pull-up resistor

INSTRUCTION SET

Definition of Symbols

SYMBOL	DEFINITION
M	Content of RAM memory location addressed by the contents of B register
←, ↔	Direction of transfer and exchange of contents
∪	Logical OR
∩	Logical AND
⊕	Exclusive OR
Aregi	The ith (i = 0 to 3) bit of A register or control register and the like
Push	Saves the contents of PC to stack register SR
Pop	Returns the contents saved in the stack register SR back to PC
Pj	Port register Pj (j = 0, 1, 2, 4, 5)
Rj	Control register other than port register. j is one or two digits hexadecimal number
PORTj	Level on port (in or out)
ROM	Indicates contents at a ROM memory location
ROM_H	Upper 4 bits of ROM content
ROM_L	Lower 4 bits of ROM content
CY	Carry signal. In this data sheet the symbol CY is used to indicate that a carry occurs at ALU. This is also expressed as CY = 1 (note that this does not mean C flag nor bit state)
x	Represents a set of bits in the operand. For example, an x in LDA x instruction denotes the 2 bits (I_1, I_0) in the operand. x may be substituted by 'y'.
reg	An abbreviation reg may follow a symbol to assure that the symbol is identified as a register. For example, Areg (or A-reg) for A register and Xreg (or X-reg) for X register to distinguish them from similar symbols or figures.

NOTES:

1. A bit of a register is specified in the position immediately following the register symbol. For example, the bit i (0, 1, 2, 3, …) of X register is expressed as Xi, that of P register is Pi, and so on.
2. Increment means binary addition of 1_H and decrement means binary addition of F_H.
3. Skipping an instruction means to ignore that instruction and to do nothing until starting the next instruction. In this sense, an instruction to be skipped is treated as an NOP instruction. Skipping 1-byte instruction requires 1-cycle, and 2-byte instruction 2-cycle. Skipping 1-byte 2-cycle instruction requires 1-cycle.
4. *SM5K7 only.

ROM Address Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TR x	80 to BF	$P_L \leftarrow x\ (I_5 - I_0)$
TL xy	E0 to E7 00 to FF	$P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
TRS x	C0 to DF	Push $P_U \leftarrow 01_H$, $P_L \leftarrow x\ (I_4 - I_0, 0)$
CALL xy	F0 to F7 00 to FF	Push $P_U \leftarrow x\ (I_{11} - I_6)$ $P_L \leftarrow y\ (I_5 - I_0)$
RTN	7D	Pop (PC ← SR)
RTNS	7E	Pop (PC ← SR), skip the return address
RTNI	7F	Pop (PC ← SR), IME ← 1
LAP1 x*	6910 to 6911	$Rx \leftarrow x\ (I_0)$

Data Load Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
LAX x	10 to 1F	$Areg \leftarrow x\ (I_3 - I_0)$
LBMX x	30 to 3F	$B_M \leftarrow x\ (I_3 - I_0)$
LBLX x	20 to 2F	$B_L \leftarrow x\ (I_3 - I_0)$
LDA x	50 to 53	$Areg \leftarrow M$, B_{M1}, $B_{M0} \leftarrow B_{M1}$ $B_{M0} \oplus x\ (I_1 - I_0)$
EXC x	54 to 57	$M \leftrightarrow Areg$, B_{M1}, $B_{M0} \leftarrow B_{M1}$ $B_{M0} \oplus x\ (I_1 - I_0)$
EXCI x	58 to 5B	$M \leftrightarrow Areg$, B_{M1}, $B_{M0} \leftarrow B_{M1}$ $B_{M0} \oplus x\ (I_1 - I_0)$, $B_L \leftarrow B_L + 1$ Skip the next step, if result of $B_L = 0_H$
EXCD x	5C to 5F	$M \leftrightarrow Areg$, B_{M1}, $B_{M0} \leftarrow B_{M1}$ $B_{M0} \oplus x\ (I_1 - I_0)$, $B_L \leftarrow B_L - 1$ Skip the next step, if result of $B_L = 0_H$
EXAX	64	$Areg \leftrightarrow Xreg$
ATX	65	$Xreg \leftarrow Areg$
EXBM	66	$B_M \leftrightarrow Areg$
EXBL	67	$B_L \leftrightarrow Areg$
EX	68	B-reg ↔ SB-reg
LAP2 x*	6912 to 6913	$B_U \leftarrow x\ (I_0)$

Arithmetic Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
ADX x	00 to 0F	Areg ← x (I_3 – I_0) + Areg, Skip the next step, if CY = 1
ADD	7A	Areg ← Areg + M
ADC	7B	Areg ← Areg + M + C, C ← CY Skip the next step, if CY = 1
COMA	79	Areg ← $\overline{\text{Areg}}$
INCB	78	B_L ← B_L + 1, Skip the next step, if result of B_L = 0_H
DECB	7C	B_L ← B_L – 1, Skip the next step, if result of B_L = $0F_H$

Test Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
TAM	6F	Skip the next step, if Areg = M
TC	6E	Skip the next step, if C = 1
TM x	48 to 4B	Skip the next step, if Mi = 1 (i = I_1, I_0)
TABL	6B	Skip the next step, if Areg = B_L
TPB x	4C to 4F	Skip the next step if Portji = 1, (j = 0, 1, 2, 3, 4, 5) (i = I_1, I_0) Skip the next step Rji = 1 (j = 08, 09, 0A, 0B, 18, 19, 1A, 1B) Skip the next step if Rji* = 1 (j = 6, 7, D, E, 0C, 0F, 1C, 1F)
TA	6C	Skip the next step, if IFA = 1, IFA ← 0
TB	6D	Skip the next step, if IFB = 1, IFB ← 0
TT1	69 02	Skip the next step, if IFT1 = 1, IFT1 ← 0
TT2	69 01	Skip the next step, if IFT2 = 1, IFT2 ← 0
TSF	69 04	Skip the next step, if IFS = 1, IFS ← 0

Bit Operation Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
SM x	44 to 47	Mi ← 1 (i = I_1, I_0)
RM x	40 to 43	Mi ← 0 (i = I_1, I_0)
SC	61	C ← 1
RC	60	C ← 0
IE	63	IME ← 1
ID	62	IME ← 0

I/O Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
INL	70	Areg ← Port3
OUTL	71	P0 ← Areg P1 ← Xreg
ANP	72	Pj ← Pj ∩ Areg (j = 0, 1, 2, 4, 5) Rj ← Rj ∩ Areg (j = 0, 3, 6, 7, D, E, 0C, 0F, 1C, 1F)
ORP	73	Pj ← Pj ∪ Areg (j = 0, 1, 2, 4, 5) Rj ← Rj ∪ Areg (j = 0, 3, 6, 7, D, E, 0C, 0F, 1C, 1F)
IN	74	A_{CC} ← Portj (j = 0, 1, 2, 3, 4, 5), Xreg, Areg ← Rj (j = 08, 09, 0A, 0B, 18, 19, 1A, 1B), Areg ← Rj (j = 6, 7, D, E, 0C, 0F, 1C, 1F)
OUT	75	Pj ← Areg (j = 0,1, 2, 4, 5), Rj ← Xreg, A_{CC} (j = 08, 09, 0B, 18, 19, 1B) Rj ← Areg (j = 3, 6, 7, D, E, 0C, 0F, 1C, 1F) R0A ← R0B, R1A ← R1B

Table Reference Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
PAT	6A	Push P_L ← (Xreg1, Xreg0, Areg) Xreg ← ROM_H, Areg ← ROM_L Pop

Divider Operation Instruction

MNE-MONIC	MACHINE CODE	OPERATIONS
DR	69 03	Divider (f_0 - f_{15}) ← 0 (divider clear)

Special Instructions

MNE-MONIC	MACHINE CODE	OPERATIONS
STOP	76	Change operation mode to STOP
HALT	77	Change operation mode to HALT
NOP	00	No operation

SYSTEM CONFIGURATION EXAMPLE

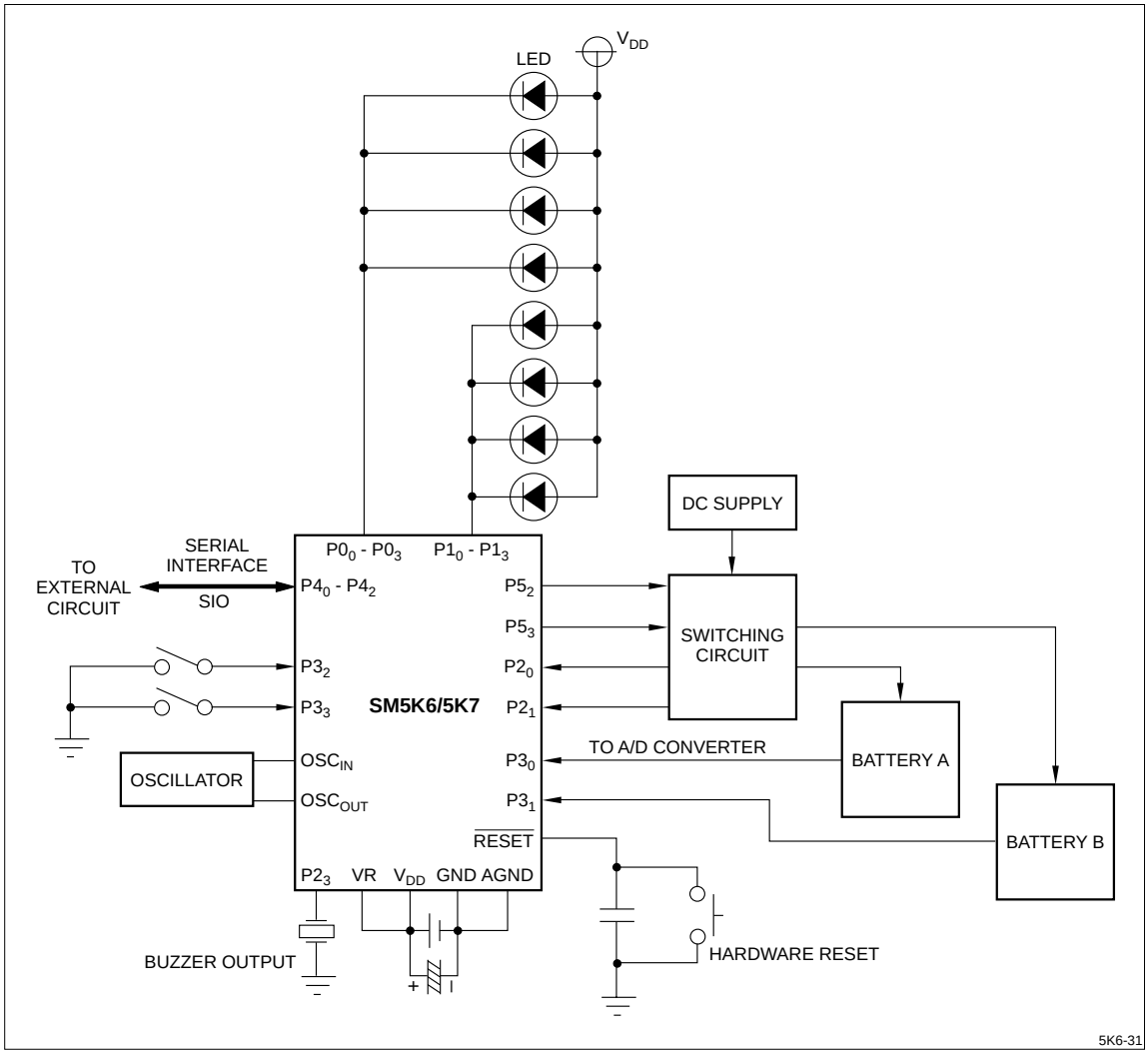


Figure 28. Example of a Versatile Charger

COMPARISON BETWEEN SM5K6 AND SM5K7

Addition of bank change over bit between ROM and RAM capacity, increase of ROM and RAM, and addition of instructions to control bank bits are major changes from SM5K6 to SM5K7. The difference between SM5K6 and SM5K7 is shown in Table 11.

Table 11. Comparison Between SM5K6 and SM5K7

	SM5K6	SM5K7
ROM capacity	4,096 bytes	8,192 bytes (4,096 bytes × 2 banks)
RAM capacity	256 × 4-bits	512 × 4-bits (256 × 4-bits × 2 banks)
Number of instructions	52 types	54 types (added two instructions for bank change)
Program counter	12-bits	13-bits (12 bits + one bit of bank change over bit)
Stack register	12-bit × 8 stages	13-bit × 8 stages
B register (RAM address pointer)	8-bits	9-bits (8-bits + one bit of bank change over bit)
SB register (Stack B register)	8-bits	9-bits
Other	DC characteristics partly changed.	

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